12/06/2002

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Dec W1
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2002/Dec W1
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2002/Nov W4
         (c) 2002 Elsevier Eng.  Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Dec W2
         (c) 2002 Inst for Sci Info
*File  34: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/Nov
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Dec W1
         (c) 2002 BLDSC all rts. reserv.
  File  94:JICST-EPlus  1985-2002/Sep W5
         (c)2002 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Oct
         (c) 2002 The HW Wilson Co.
  File 144:Pascal  1973-2002/Dec W1
         (c) 2002 INIST/CNRS
  File 305:Analytical Abstracts  1980-2002/Nov W4
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Nov
         (c) 2002 DECHEMA
  File  96:FLUIDEX  1972-2002/Nov
         (c) 2002 Elsevier Science Ltd.
  File 103:Energy SciTec  1974-2002/Nov B2
         (c) 2002 Contains copyrighted material
*File 103: For access restrictions see Help Restrict.
```

12/06/2002

Set	Items	Description
S1	192116	ALUMINATE OR (ALUMINUM OR AL)(W)(OXIDE OR O) OR AL2O3 OR RUBY OR SAPPHIRE OR LEUCOSAPPHIRE
S2	5854	CI=(AL SS(S) O SS)(S)NE=2
S3	26395	Y2O3 OR (Y OR YTTRIUM)(W)(OXIDE OR O) OR DIYTTRIUM(W)TRIOXIDE OR NANOTEK OR YTTRIUM(W)SESQUIOXIDE OR CI=(Y SS(S) O SS)(S)NE=2
S4	665	ZRSI(W)O OR SILICON(W)ZIRCONIUM(W)OXIDE OR CI=(SI SS(S) ZR SS(S) O SS)(S)NE=3
S5	34	ZR(W)SI(W)O
S6	236	HF(W)SI(W)O OR HAFNIUM(W)SILICON(W)OXIDE OR HAFNIUM(W)ALLOY OR CI=(SI SS(S) HF SS(S) O SS)(S)NE=3
S7	9083	LA2O3 OR (LA OR LANTHANUM)(W)(OXIDE OR O) OR (DILANTHANUM OR LANTHANUM)(W)(OXIDE OR TRIOXIDE) OR CI=(LA SS(S) O SS)(S)NE=2
S8	36583	ZRO2 OR (ZR OR ZIRCONIUM)(W)(OXIDE OR O) OR SUPEROXIDO(W)(ZIRCONIUM OR ZR) OR BADDELEYITE OR CI=(ZR SS(S) O SS)(S)NE=2
S9	1	SUPEROXID?(W)(ZIRCONIUM OR ZR)
S10	2582	HFO2 OR (HF OR HAFNIUM)(W)(OXIDE OR O OR DIOXIDE) OR HAFNOTRAST OR CI=(HF SS(S) O SS)(S)NE=2
S11	1547	PR2O3 OR (PRASEODYMIUM OR PR)(W)(OXIDE OR O OR SESQUIOXIDE OR TRIOXIDE) OR PRASEODYMIA OR CI=(PR SS(S) O SS)(S)NE=2
S12	84176	TIO2 OR (TI OR TITANIUM)(W)(OXIDE OR O) OR RUTILE OR SAGENITE OCTAHEDRITE OR CI=(TI SS(S) O SS)(S)NE=2
S13	540767	SIO2 OR (SILICON OR SI)(W)(DIOXIDE OR O2) OR SILICA OR MYRICKITE OR TRIDYMITE OR BOBKOVITE OR MOGANITE OR QUARTZ OR CRISTOBALITE OR ADELITE OR ACTICEL
S14	10051	ACEMATT OR STISHOVITE OR COESITE OR SIBELITE OR CRYSVARL OR CRYSTOBALITE OR SARDONYX OR QUARTZINE OR SIKRON OR MILLISIL OR ROCK(W)CRYSTAL OR CI=(SI SS(S) O SS)(S)NE=2
S15	3993	FLASH(2N)(MEMORY OR RAM)
S16	2056	FLASH(2N)MEMORIES
S17	135	(S15 OR S16) AND (S1:S14)
S18	94	RD (unique items)
S19	1	S18 AND DRAIN? ? AND SOURCE
S20	38	S18 AND (DIELECTRIC OR OXIDE OR INSULAT?)(3N)(FILM? OR LAYER? OR COAT?)
S21	11	(S15 OR S16) AND (S1:S12)
S22	10	S21 NOT S20
S23	39	S19 OR S20
S24	49	S18 NOT (S19 OR S20 OR S21)

12/06/2002

22/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6980848 INSPEC Abstract Number: B2001-08-1265D-018, C2001-08-5320Z-002
Title: Stack gate PZT/Al/sub 2/O/sub 3/ one transistor ferroelectric memory
Author(s): Chin, A.; Yang, M.Y.; Sun, C.L.; Chen, S.Y.
Author Affiliation: Dept. of Electron. Eng., Nat. Chiao Tung Univ., Hsinchu, Taiwan
Journal: IEEE Electron Device Letters vol.22, no.7 p.336-8
Publisher: IEEE,
Publication Date: July 2001 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200107)22:7L.336:SGAT;1-B
Material Identity Number: I338-2001-007
U.S. Copyright Clearance Center Code: 0741-3106/2001/$10.00
Language: English
Abstract: We have developed a single transistor ferroelectric memory using stack gate PZT/Al/sub 2/O/sub 3/ structure. For the same ~40 AA dielectric thickness, the PZT/Al/sub 2/O/sub 3//Si gate dielectric has much better C-V characteristics and larger threshold voltage shift than those of PZT/SiO/sub 2//Si. Besides, the ferroelectric MOSFET also shows a large output current difference between programmed on state and erased off state. The <100 us erase time is much faster than that of **flash memory** where the switching time is limited by erase time.
Subfile: B C

22/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5256230 INSPEC Abstract Number: A9611-9385-038, B9606-7710D-040
Title: A new family of real-time wave and tide instruments
Author(s): Trageser, J.I.
Author Affiliation: InterOcean Systems Inc., San Diego, CA, USA
Conference Title: `Challenges of Our Changing Global Environment`. Conference Proceedings. OCEANS `95 MTS/IEEE (Cat. No.95CH35870) Part vol.3 p.1760-8 vol.3
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 3 vol. (xxxxiii+xxxvii+2103) pp.
ISBN: 0 933957 14 9 Material Identity Number: XX95-03107
Conference Title: `Challenges of Our Changing Global Environment`. Conference Proceedings. OCEANS `95 MTS/IEEE
Conference Sponsor: Marine Technol. Soc.; OES; IEEE
Conference Date: 9-12 Oct. 1995 Conference Location: San Diego, CA, USA
Language: English
Abstract: A series of compact, intelligent instruments were developed as a low-cost solution to the needs of marine scientists and engineers for measurement of nondirectional wave characteristics as well as tides. The design of these instruments varies from a pressure sensor connected to a laptop PC to a self contained instrument consisting of a precision silicon-on-**sapphire** pressure sensor, 32 bit microprocessor, and **flash memory** . In the first case the data collection and wave analysis are controlled by software running on the remote computer. In the second case, the same wave processing algorithms are contained in firmware

of the internal 32 bit microprocessor. The instruments output one minute tide averages, wave statistics, and 62 spectral surface energy components for wave periods from 3 seconds to 30 seconds. A description of the instrument design is presented along with the theory of operation and a discussion of the algorithms chosen for the processing of the wave statistics. The mooring arrangements used off the San Diego coast for inter comparison studies is described. Two of the new instruments were deployed along with an S4ADW directional wave current meter. The data and processing methods from all three instruments are compared to the wave statistics data obtained from the single-point wave gauge located at the Scripps Pier in La Jolla, CA which is installed and operated under the Coastal Data Information Program by the Scripps Institute of Oceanography.
Subfile: A B

22/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06101152
E.I. No: EIP02307034395
Title: **Sapphire** - A JavaCard VM for a 1-MB **flash memory** smart card
Author: Suzuki, Katsuhiko; Hirata, Shinichi; Yamamoto, Shuichiro
Source: NTT Review v 14 n 1 January 2002. p 20-22
Publication Year: 2002
CODEN: NTTREK ISSN: 0915-2334
Language: English
Abstract: The most critical problem with JavaCards in the limited memory capacity of smart cards. Although JavaCard VM can handle multiple applications, the smaller the smart card memory, the fewer applets it can run. The **Sapphire** is designed to resolve this issue, providing a large **flash memory** capacity of 1 Mbyte.

22/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04352492
E.I. No: EIP96023040505
Title: New family of real-time wave & tide instruments
Author: Trageser, James H.
Corporate Source: InterOcean Systems, Inc, San Diego, CA, USA
Conference Title: Proceedings of the 1995 IEEE/MTS Oceans Conference. Part 3 (of 3)
Conference Location: San Diego, CA, USA Conference Date: 19951009-19951012
E.I. Conference No.: 44345
Source: Oceans Conference Record (IEEE) v 3 1995. IEEE, Piscataway, NJ, USA,95CB35870. p 1760-1768
Publication Year: 1995
CODEN: OCNSDK ISSN: 0197-7385
Language: English
Abstract: A series of compact, intelligent instruments were developed as low-cost solution for measurement of non-directional wave characteristics as well as tides. The instruments' design varies from a pressure sensor connected to a laptop PC to a self-contained instrument consisting of a precision silicon-on-**sapphire** pressure sensor, 32-bit microprocessor, and **flash memory**. In the first case the data collection and

wave analysis are controlled by software running on the remote computer. In the second, the same wave processing algorithms are contained in firmware of the internal 32-bit microprocessor. A description of the instrument design is presented along with the theory of operation and a discussion of the algorithms chosen for the processing of the wave statistics. The mooring arrangements used off the San Diego coast for inter-comparison studies is described. 5 Refs.

22/3,AB/5 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10733374 Genuine Article#: 562UV Number of References: 0
Title: **Sapphire** - A JavaCard VM for a 1-MB **flash memory** smart card (ABSTRACT AVAILABLE)
Author(s): Suzuki K (REPRINT) ; Hirata S; Yamamoto S
Corporate Source: Nippon Telegraph & Tel Publ Corp,NTT Informat Sharing Platform Labs, Chiyoda Ku,1-6 Uchishiwai Cho,1 Chome/Tokyo 100//Japan/ (REPRINT); Nippon Telegraph & Tel Publ Corp,NTT Informat Sharing Platform Labs, Chiyoda Ku,Tokyo 100//Japan/
Journal: NTT REVIEW, 2002, V14, N1 (JAN), P20-22
ISSN: 0915-2334 Publication date: 20020100
Publisher: NTT CORP, 1-6 UCHISAIWAI-CHO 1 CHOME, CHIYODA-KU, TOKYO, 100, JAPAN
Language: English Document Type: ARTICLE
Abstract: The most critical problem with JavaCards is the limited memory capacity of smart cards. Although JavaCard VM can handle multiple applications, the smaller the smart card memory, the fewer applets it can run. The **Sapphire** is designed to resolve this issue, providing a large **flash memory** capacity of 1 Mbyte.

22/3,AB/6 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09763421 Genuine Article#: 445HR Number of References: 13
Title: Stack gate PZT/**Al2O3** one transistor ferroelectric memory (ABSTRACT AVAILABLE)
Author(s): Chin A (REPRINT) ; Yang MY; Sun CL; Chen SY
Corporate Source: Natl Chiao Tung Univ,Dept Elect Engn,Hsinchu 300//Taiwan/ (REPRINT); Natl Chiao Tung Univ,Dept Elect Engn,Hsinchu 300//Taiwan/; Natl Chiao Tung Univ,Dept Mat Sci & Engn,Hsinchu 300//Taiwan/
Journal: IEEE ELECTRON DEVICE LETTERS, 2001, V22, N7 (JUL), P336-338
ISSN: 0741-3106 Publication date: 20010700
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: We have developed single transistor ferroelectric memory using stack gate PZT/**Al2O3** structure. For the same similar to 40 Angstrom dielectric thickness, the PZT/**Al2O3**/Si gate dielectric has much better C-V characteristics and larger threshold voltage shift than those of PZT/SiO2/Si. Besides, the ferroelectric MOSFET also shows a large output current difference between programmed on state and erased off state, The <100 ns erase time is much faster than that of **Flash memory** where the switching time is limited by erase time.

22/3,AB/7 (Item 1 from file: 94)

12/06/2002

DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

05081849 JICST ACCESSION NUMBER: 02A0178186 FILE SEGMENT: JICST-E
Smart Card Information Sharing Platform. **Sapphire**. A JavaCard VM for a 1-MB **Flash Memory** Smart Card.
SUZUKI K (1); HIRATA S (1); YAMAMOTO S (1)
(1) Ntt Corp.
NTT Rev, 2002, VOL.14,NO.1, PAGE.20-22, FIG.4
JOURNAL NUMBER: F0282BAW ISSN NO: 0915-2334
UNIVERSAL DECIMAL CLASSIFICATION: 681.32.07 681.3.06 681.327
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The most critical problem with JavaCards is the limited memory capacity of smart cards. Although JavaCard VM can handle multiple applications, the smaller the smart card memory, the fewer applets it can run. The **Sapphire** is designed to resolve this issue, providing a large **flash memory** capacity of 1 Mbyte. (author abst.)

22/3,AB/8 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

04858879 JICST ACCESSION NUMBER: 01A0340324 FILE SEGMENT: JICST-E
Implementation and evaluation of JavaCard "**Sapphire**" designed for SmartCard with **flash memory**.
HIURA YUJI (1); SUZUKI KATSUHIKO (1); YOSHIDA SHINSUKE (1)
(1) Nippon Telegraph and Telephone Corp. (NTT), Information Sharing Platform Lab., JPN
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2001, VOL.100,NO.541(KBSE2000 54-65), PAGE.9-16, FIG.9, TBL.2, REF.8
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.06 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: High performance and multi-purpose SmartCard was realized and various service developments being expected. "**Sapphire**" is a JavaCard which is the multi-application environment on SmartCard implemented with a mass **flash memory** (1MB). But there is a problem that the access speed to the memory decreases in the case of frequently being updated to data, because **flash memory** isn't fully bit-alterable. In this paper, we report on the speed-up and optimization technology of **flash memory** management on SmartCard by adaptation of the characteristic of JavaCard. (author abst.)

22/3,AB/9 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

15686909 PASCAL No.: 02-0394410
Sapphire - A JavaCard VM for a 1-MB **flash memory** smart card

12/06/2002

SUZUKI K; HIRATA S; YAMAMOTO S
Journal: NTT Review, 2002, 14 (1) 20-22
Language: English
The most critical problem with JavaCards in the limited memory capacity of smart cards. Although JavaCard VM can handle multiple applications, the smaller the smart card memory, the fewer applets it can run. The **Sapphire** is designed to resolve this issue, providing a large **flash memory** capacity of 1 Mbyte.

22/3,AB/10 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

15151088 PASCAL No.: 01-0314398
Stack gate PZT/**Al2O3** one transistor ferroelectric memory
CHIN A; YANG M Y; SUN C L; CHEN S Y
Department of Electronics Eng. National Chiao Tung University, Hsinchu 300, Taiwan
Journal: IEEE Electron Device Letters, 2001, 22 (7) 336-338
Language: English
We have developed single transistor ferroelectric memory using stack gate PZT/**Al2O3** structure. For the same Degree similar to<pilcrow>40 A dielectric thickness, the PZT/**Al2O3** /Si gate dielectric has much better C-V characteristics and larger threshold voltage shift than those of PZT/SiO2/Si. Besides, the ferroelectric MOSFET also shows a large output current difference between programmed on state and erased off state. The <100 ns erase time is much faster than that of **Flash memory** where the switching time is limited by erase time.

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7432308 INSPEC Abstract Number: B2002-12-1265D-063, C2002-12-5320G-046
Title: Multi-level vertical channel SONOS nonvolatile memory on SOI
Author(s): Yong Kyu Lee; Suk Kang Sung; Jae Seong Sim; Chang Ju Lee; Tae Hun Kim; Sang Hun Lee; Jong Duk Lee; Byung Gook Park; Dong Hun Lee; Young Wuk Kim
Author Affiliation: Inter-university Semicond. Res. Center, Seoul Nat. Univ., South Korea
Conference Title: 2002 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.01CH37303) p.208-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xii+228 pp.
ISBN: 0 7803 7312 X Material Identity Number: XX-2002-01941
U.S. Copyright Clearance Center Code: 0-7803-7312-X/02/$17.00
Conference Title: 2002 Symposium on VLSI Technology Digest of Technical Papers
Conference Date: 11-13 June 2002 Conference Location: Honolulu, HI, USA
Language: English
Abstract: A new VC-SONOS (vertical channel SONOS) memory cell structure is proposed and fabricated using a 0.12 mu m SOI standard logic process for a next generation **flash memory** cell with ultra high density. This fabricated VC-SONOS memory cell, which has 57 nm wide vertical channels and 15 AA tunnel gate oxide, shows not only scaling breakthrough beyond 0.10 mu m **flash memory** but also multi-level operation with negative programming voltages.
Subfile: B C

23/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6754166 INSPEC Abstract Number: B2000-12-2530F-044
Title: Impact of electrical stress on hot-electron injection in ultra-thin SiO/sub 2/ films
Author(s): Okhonin, S.; Berk, Y.; Ils, A.; Fazan, P.; Guegan, G.; Deleonibus, S.; Martin, F.
Author Affiliation: Inst. for Micro- and Optoelectron., Swiss Federal Inst. of Technol., Lausanne, Switzerland
Conference Title: ESSDERC'99. Proceedings of the 29th European Solid-State Device Research Conference p.588-91
Editor(s): Maes, H.E.; Mertens, R.P.; Declerck, G.; Grunbacher, H.
Publisher: Editions Frontieres, Neuilly sur Seine, France
Publication Date: 1999 Country of Publication: France xv+743 pp.
ISBN: 2 86332 245 1 Material Identity Number: XX-1999-03616
Conference Title: ESSDERC'99. Proceedings of the 29th European Solid-State Device Research Conference
Conference Sponsor: IEEE; IMEC
Conference Date: 13-15 Sept. 1999 Conference Location: Leuven, Belgium
Language: English
Abstract: Hot electron injection from the silicon substrate into ultra-thin SiO/sub 2/ layers is investigated before and after an electrical stress. It is shown that the hot electron tunneling increases after Fowler-Nordheim injection similar to the normally measured stress-induced-leakage effect. In contrast the hot-electron emission over

the silicon/**silicon dioxide** barrier is lower after the same stress. This is due to the high sensitivity of hot electron emission to the stress-induced negative charge in the oxide. The studied effects are particularly important to understanding of the mechanisms of **flash memory** degradation.
Subfile: B

23/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6417976 INSPEC Abstract Number: B2000-01-1265D-010
Title: Off-stochiometric silicon oxides for applications in low-voltage **flash memories**
Author(s): Irrera, F.; Russo, F.
Author Affiliation: Dipt. di Ingegneria Elettronica, Rome Univ., Italy
Journal: Microelectronic Engineering Conference Title: Microelectron. Eng. (Netherlands) vol.48, no.1-4 p.423-6
Publisher: Elsevier,
Publication Date: Sept. 1999 Country of Publication: Netherlands
CODEN: MIENEF ISSN: 0167-9317
SICI: 0167-9317(199909)48:1/4L.423:SSOA;1-X
Material Identity Number: F621-1999-006
U.S. Copyright Clearance Center Code: 0167-9317/99/$20.00
Conference Title: 11th Biennial Conference on Insulating Films on Semiconductors
Conference Date: 16-19 June 1999 Conference Location: Koster Banz, Germany
Language: English
Abstract: In this paper we systematically investigate the mechanism of enhanced Fowler-Nordheim injection in a MOS capacitor under accumulation when a film of off-stochiometric silicon oxide is deposited between the polygate and the thermal **silicon dioxide**. Experimental results prompt for application in low-voltage **flash memories**.
Subfile: B

23/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6330214 INSPEC Abstract Number: B1999-10-1265D-004
Title: 2-dimensional simulation of FN current suppression including phonon assisted tunneling model in **silicon dioxide**
Author(s): Eikyu, K.; Sakakibara, K.; Ishikawa, K.; Nishimura, T.
Author Affiliation: ULSI Dev. Center, Mitsubishi Electr. Corp., Itami, Japan
Journal: IEICE Transactions on Electronics vol.E82-C, no.6 p.889-93
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: June 1999 Country of Publication: Japan
CODEN: IELEEJ ISSN: 0916-8524
SICI: 0916-8524(199906)E82C:6L.889:DSCS;1-2
Material Identity Number: P712-1999-007
Language: English
Abstract: A gate oxide excess current model is described, based on the phonon-assisted tunneling process of electrons into neutral traps. The influence on the local electric field of the charge of electrons trapped by neutral traps in the gate oxide is simulated using a two-dimensional device

simulator into which the new model is incorporated. Fowler-Nordheim (FN) current is suppressed with an increase in the neutral trap density to over 10/sup 19/ cm/sup -3/. The calculated results reflect the endurance characteristics of **flash memories** in which erase/write operation speed depends on FN current.
Subfile: B

23/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5938956 INSPEC Abstract Number: B9807-2570F-006
Title: Charging and intrinsic-leakage current peaks in thin **silicon-dioxide** films
Author(s): Yamada, R.; Yugami, J.; Ohkura, M.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Tokyo, Japan
Conference Title: 1997 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.97CH36114) p.147-8
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1997 Country of Publication: Japan xv+162 pp.
ISBN: 4 930813 75 1 Material Identity Number: XX98-00123
Conference Title: Proceedings of 1997 Symposium on VLSI Technology
Conference Date: 10-12 June 1997 Conference Location: Kyoto, Japan
Language: English
Abstract: A new leakage mode in thin SiO/sub 2/ films which may affect the retention characteristics of **flash memories** is examined. To improve the reliability of **flash memories** , electrical properties of the gate oxide were studied by using MOS capacitors. Since a transient current as well as a steady current is observed in a MOS capacitor under a constant gate bias, the time dependence of the current was measured to separate these currents. Through this operation, current peaks were found in both the transient and the steady current dependences on the gate bias. The peak for the transient current can be explained by resonant tunneling through traps near the oxide interface, and that for the steady current can be attributed to resonant tunneling leakage through traps distributed in the bulk oxide. The latter mechanism is a form of intrinsic leakage that affects the retention characteristics, and thus it should be considered in designing **flash memories**.
Subfile: B

23/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5802215 INSPEC Abstract Number: B9802-1265D-031
Title: A 0.24- mu m/sup 2/ cell process with 0.18- mu m width isolation and 3-D interpoly **dielectric films** for 1-Gb **flash memories**
Author(s): Kobayashi, T.; Mastsuzaki, N.; Sato, A.; Katayama, A.; Kurata, H.; Miura, A.; Mine, T.; Goto, Y.; Morimoto, T.; Kume, H.; Kure, T.; Kimura, K.
Author Affiliation: Central Res. Lab., Hitachi Ltd., Kokubunji, Japan
Conference Title: International Electron Devices Meeting 1997. IEDM Technical Digest (Cat. No.97CH36103) p.275-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 944 pp.
ISBN: 0 7803 4100 7 Material Identity Number: XX97-03283

U.S. Copyright Clearance Center Code: 0 7803 4100 7/97/$10.00
Conference Title: International Electron Devices Meeting. IEDM Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 7-10 Dec. 1997 Conference Location: Washington, DC, USA
Language: English
Abstract: We have developed a 0.24- mu m/sup 2/ contactless-array **flash memory** cell by using 0.2- mu m process technology. For reducing the data line pitch, a 0.18- mu m-wide self-aligned shallow groove isolation (SGI) is formed between memory cells, by filling the grooves with boron phosphosilicate glass (BPSG), to maintain the isolation breakdown voltage. In addition, three-dimensional (3-D) CVD SiO/sub 2/ single-**layer** interpoly **dielectric films** with high capacitance are employed to decrease the internal operating voltage by increasing the coupling ratio. These processes are the keys to fabricating 1-Gb **flash memory** cells.
Subfile: B

23/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5573802 INSPEC Abstract Number: B9706-2550E-049
Title: Influence of carbon contamination on ultra thin gate oxide reliability
Author(s): Iwamoto, T.; Miyake, T.; Ohmi, T.
Author Affiliation: Dept. of Electron. Eng., Tohoku Univ., Sendai, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2875 p.207-15
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1996 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2875L.207:ICCU;1-P
Material Identity Number: C574-96227
U.S. Copyright Clearance Center Code: 0 8194 2273 8/96/$6.00
Conference Title: Microelectronic Device and Multilevel Interconnection Technology II
Conference Sponsor: SPIE
Conference Date: 16-17 Oct. 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: When an Si wafer is transported after the gate oxidation process, the gate oxide surface is exposed to the clean room air, and hydrocarbons in the clean room air adhere to the gate oxide surface. In this paper, we demonstrate that the carbon contamination caused by wafer exposure to the clean room air induces degradation of the gate oxide reliability, and we have improved the gate oxide performance by using a closed system, where the oxidation is followed by in-situ phosphorus-doped polysilicon gate formation. Carbon contamination is a serious problem for gate **oxide films** used under high electric field conditions, such as a tunnel oxide for **flash memories**.
Subfile: B

23/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

4963125 INSPEC Abstract Number: B9507-2550E-040
Title: Characterization of PECVD Si/sub x/O/sub y/N/sub z/:H films and its correlation to device performance and reliability
Author(s): Moinpour, M.; Mack, K.; Cham, J.; Moghadam, F.; Williams, B.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Conference Title: Materials Reliability in Microelectronics IV. Symposium p.75-82
Editor(s): Borgesen, P.; Coburn, J.C.; Sanchez, J.E., Jr.; Rodbell, K.P.; Filter, W.F.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA xv+630 pp.
Conference Title: Materials Reliability in Microelectronics IV. Symposium
Conference Date: 5-8 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: For integrated circuits, the integrity and film quality of the final passivation layer plays an important role in device performance and reliability. Hydrogenated amorphous silicon oxynitride (alpha -Si/sub x/N/sub **y/O** /sub z/:H) films deposited by plasma enhanced chemical vapor deposition (PECVD) have been extensively used for final device passivation applications. In this paper, a detailed characterization of the PECVD oxynitride process for 200 mm Si wafer processing is presented. Silicon oxynitride of various compositions were deposited by changing the amounts of silane, ammonia, nitrogen and nitrous oxide in the reactant gas stream. Ultraviolet/visible (UV/VIS) spectroscopy, Fourier transform infrared (FTIR) spectroscopy, Rutherford backscattering spectrometry (RBS), and refractive index measurements were used to examine the variation in physical, optical and electrical properties. A correlation is observed between the oxynitride film composition, mainly the N-H/Si-H ratio, and UV transmissivity (UV %T) which is of particular interest for memory applications. Effects of oxynitride film quality on e-test parameters and device performance are discussed.
Subfile: B

23/3,AB/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05954539
E.I. No: EIP01506759962
Title: Microelectronic engineering
Author: Sangiorgi, E. (Ed.); Semi, L. (Ed.)
Conference Title: 12th Biannual Conference on Insulating Films on Semi-Conductors (INFOS 2001)
Conference Location: Udine, Italy Conference Date: 20010620-20010623
E.I. Conference No.: 58721
Source: Microelectronic Engineering v 59 n 1-4 November 2001. 510p
Publication Year: 2001
CODEN: MIENEF ISSN: 0167-9317
Language: English
Abstract: The proceedings contains 73 papers from the Conference on Microelectronic Engineering. The topics discussed include: carrier transport properties of thin gate oxides after soft and hard breakdown; current noise at oxide hard breakdown; electron trap generation in gate oxides; a two-trap tunneling model for stress-induced leakage currents (SILC) in **flash memories**; and reversed electron-hole pair transport in silicon on insulator (SOI) structures. (Edited abstract)

23/3,AB/10 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05378649
E.I. No: EIP99104816859
Title: Non-volatile MOSFET memory device based on mobile protons in SiO//2 thin films
Author: Vanheusden, K.; Warren, W.L.; Devine, R.A.B.; Fleetwood, D.M.; Draper, B.L.; Schwank, J.R.
Corporate Source: US Air Force Research Lab, Kirtland Air Force Base, NM, USA
Conference Title: Proceedings of the 1998 2nd International Conference on Amorphous and Crystalline Insulating Thin Films II
Conference Location: Hong Kong, China Conference Date: 19981012-19981014
E.I. Conference No.: 55673
Source: Journal of Non-Crystalline Solids v 254 1999. p 1-10
Publication Year: 1999
CODEN: JNCSBJ ISSN: 0022-3093
Language: English
Abstract: It is shown how mobile H** plus ions can be generated thermally inside the **oxide layer** of Si/SiO//2/Si structures. The technique involves only standard silicon processing steps: the non-volatile field effect transistor (NVFET) is based on a standard MOSFET with thermally grown SiO//2 capped with a poly-silicon **layer**. The capped thermal **oxide** receives an anneal at approximately 1100 degree C that enables the incorporation of the mobile protons into the gate oxide. The introduction of the protons is achieved by a subsequent 500-800 degree C anneal in a hydrogen-containing ambient, such as forming-gas (N//2:H//2 95:5). The mobile protons are stable and entrapped inside the **oxide layer**, and unlike alkali ions, their space-charge distribution can be controlled and rearranged at room temperature by an applied electric field. Using this principle, a standard metal-oxide-semiconductor (MOS) transistor can be converted into a non-volatile memory transistor that can be switched between `normally on' and `normally off'. Switching speed, retention, endurance, and radiation tolerance data are presented showing that this non-volatile memory technology can be competitive with existing Si-based non-volatile memory technologies such as the floating gate technologies (e.g. **Flash memory**). (Author abstract) 23 Refs.

23/3,AB/11 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05320206
E.I. No: EIP99074721616
Title: Properties of stacked **dielectric films** composed of SiO//2/Si//3N//4/SiO//2
Author: Santucci, S.; Lozzi, L.; Passacantando, M.; Phani, A.R.; Palumbo, E.; Bracchitta, G.; De Tommasis, R.; Torsi, A.; Alfonsetti, R.; Moccia, G.
Corporate Source: Universita dell'Aquila, L'Aquila, Italy
Conference Title: Proceedings of the 1998 2nd Franco-Italian Symposium on SiO(2) and Advanced Dielectrics
Conference Location: L'Aquila, Italy Conference Date: 19980615-19980617
E.I. Conference No.: 55179
Source: Journal of Non-Crystalline Solids v 245 1999. p 224-231
Publication Year: 1999
CODEN: JNCSBJ ISSN: 0022-3093

Language: English
Abstract: **Dielectric films** composed of silicon **oxide** -nitride-oxide (ONO) structure have been grown over a polycrystalline silicon phosphorous-doped substrate. The films with a total thickness of about 30 nm have been obtained by two different deposition techniques of the top-**oxide layer** i.e. thermal oxidation of the nitride layers and low pressure chemical vapour deposition, while the bottom **oxide** and the nitride **layer** were obtained by thermal oxidation and low pressure chemical vapour deposition, respectively. The chemical composition was measured by XPS Auger parameter technique while the thickness of the deposited layers was determined by the X-ray reflectivity method and compared with the measurements performed on transmission electron microscopy cross-section images. The influence of the layer composition and thickness on the electrical properties of the whole **film**, used as **dielectric layer** of a capacitor with doped polycrystalline silicon as electrodes, have been investigated by measuring current as a function of voltage to study the mechanisms which contribute to an increase of the leakage current with increasing applied voltage. Furthermore, electrical erasable programmable read-only **flash memory** devices built using these **dielectric layers** in the floating gate structure have been measured for `data retention loss' after thermal stress. The results give a complete picture on the role of the two topmost layers of the ONO structure towards the electrical behaviour. (Author abstract) 18 Refs.

23/3,AB/12 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04913709
E.I. No: EIP98014030129
Title: Protonic nonvolatile field effect transistor memories in Si/SiO//2/Si structures
Author: Warren, W.L.; Fleetwood, D.M.; Schwank, J.R.; Shaneyfelt, M.R.; Draper, B.L.; Winokur, P.S.; Knoll, M.G.; Vanheusden, K.; Devine, R.A.B.; Archer, L.B.; Wallace, R.M.
Corporate Source: Sandia Natl Lab, Albuquerque, NM, USA
Conference Title: Proceedings of the 1997 IEEE Nuclear and Space Radiation Effects Conference, NSREC. Part 1 (of 3)
Conference Location: Snowmass Village, CO, USA Conference Date: 19970721-19970725
E.I. Conference No.: 47658
Source: IEEE Transactions on Nuclear Science v 44 n 6 pt 1 Dec 1997. p 1789-1798
Publication Year: 1997
CODEN: IETNAE ISSN: 0018-9499
Language: English
Abstract: A low-voltage, radiation-tolerant, nonvolatile field effect transistor (NVFET) memory involving proton motion in SiO//2 is illustrated in both bulk Si and silicon-on-insulator devices. We discuss a mechanism by which the protons are created in the **oxide layer** by a forming gas anneal. At low temperature (T less than 250 degree C), the H** plus is largely `imprisoned' in the buried SiO//2 layer; i.e., the ions are sandwiched between the two encapsulating Si layers. The Si layers can be either c-Si or poly-Si, thus the technology is compatible with standard Si processing. The protons can be reliably and controllably drifted from one interface to another without any noticeable degradation in the signal past 10**6 cycles. Under an unbiased condition, the net proton density is not significantly affected by radiation up to at least 100 krad (SiO//2). Last, we compare many of the properties of the NVFET to commercial **flash**

nonvolatile **memories**. (Author abstract) 34 Refs.

23/3,AB/13 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11119099 Genuine Article#: 609ZA Number of References: 9
Title: Location of holes in silicon-rich oxide as memory states (ABSTRACT AVAILABLE)
Author(s): Crupi I (REPRINT) ; Lombardo S; Rimini E; Gerardi C; Fazio B; Melanotte M
Corporate Source: Univ Catania,Dept Phys,Corso Italia 57/I-95129 Catania//Italy/ (REPRINT); Univ Catania,Dept Phys,I-95129 Catania//Italy/; Univ Catania,INFM,I-95129 Catania//Italy/; CNR,IMM,I-95121 Catania//Italy/; STMicroelectronics,C R&D,I-95121 Catania//Italy/
Journal: APPLIED PHYSICS LETTERS, 2002, V81, N19 (NOV 4), P3591-3593
ISSN: 0003-6951 Publication date: 20021104
Publisher: AMER INST PHYSICS, CIRCULATION & FULFILLMENT DIV, 2 HUNTINGTON QUADRANGLE, STE 1 N O 1, MELVILLE, NY 11747-4501 USA
Language: English Document Type: ARTICLE
Abstract: The induced changes of the flatband voltage by the location of holes in a silicon-rich **oxide** (SRO) **film** sandwiched between two thin **SiO2 layers** [used as gate **dielectric** in a metal-oxide-semiconductor (MOS) capacitor] can be used as the two states of a memory cell. The principle of operation is based on holes permanently trapped in the SRO layer and reversibly moved up and down, close to the metal and the semiconductor, in order to obtain the two logic states of the memory. The concept has been verified by suitable experiments on MOS structures. The device exhibits an excellent endurance behavior and, due to the low mobility of the holes at low field in the SRO layer, a much longer refresh time compared to conventional dynamic random access memory cells. (C) 2002 American Institute of Physics.

23/3,AB/14 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10316158 Genuine Article#: 511RT Number of References: 17
Title: Radiation damage in **flash memory** cells (ABSTRACT AVAILABLE)
Author(s): Claeys C (REPRINT) ; Ohyama H; Simoen E; Nakabayashi M; Kobayashi K
Corporate Source: Katholieke Univ Leuven,EE Dept,Kasteelplein 10/B-3001 Louvain//Belgium/ (REPRINT); IMEC,B-3001 Louvain//Belgium/; KNCT,Kumamoto 8611102//Japan/; Mitsubishi Electr Corp,Kumamoto 8611197//Japan/; NEC IC Microcomp Syst,Kumamoto 8612201//Japan/
Journal: NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH SECTION B-BEAM INTERACTIONS WITH MATERIALS AND ATOMS, 2002, V186 (JAN), P392-400
ISSN: 0168-583X Publication date: 20020100
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE
Abstract: Results are presented of a study on the effects of total ionization dose and displacement damage, induced by high-energy electrons, protons and alphas, on the performance degradation of **flash memory** cells integrated in a microcomputer. A conventional stacked-gate n-channel **flash memory** cell using a 0.8 mum n-polysilicon gate technology is employed. Irradiations by

1-MeV electrons and 20-MeV protons and alpha particles were done at room temperature. The impact of the fluence on the input characteristics, threshold voltage shift and drain and gate leakage, as investigated. The threshold voltage change for proton and alpha irradiations is about three orders of magnitude larger than that for electrons. The performance degradation is mainly caused by the total ionization dose (TID) damage in the tunnel oxide and in the interpoly **dielectric layer** and by the creation of interface traps at the Si -**SiO2** interface. The impact of the irradiation temperature on the device degradation was studied for electrons and gammas, pointing out that irradiation at room temperature is mostly the worst case. Finally, attention is given to the impact of isochronal and isothermal annealing on the recovery of the degradation introduced after room temperature proton and electron irradiation.

23/3,AB/15 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09617069 Genuine Article#: 428AF Number of References: 25
Title: Electrical and structural characterization of metal-oxide-semiconductor capacitors with silicon rich oxide (ABSTRACT AVAILABLE)
Author(s): Crupi I (REPRINT) ; Lombardo S; Spinella C; Bongiorno C; Liao Y; Gerardi C; Fazio B; Vulpio M; Privitera S
Corporate Source: CNR,IMETEM,Stradale Primosole 50/I-95121 Catania//Italy/ (REPRINT); CNR,IMETEM,I-95121 Catania//Italy/; STMicroelect,I-95121 Catania//Italy/; Univ Catania,Dept Phys,I-95129 Catania//Italy/
Journal: JOURNAL OF APPLIED PHYSICS, 2001, V89, N10 (MAY 15), P5552-5558
ISSN: 0021-8979 Publication date: 20010515
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501 USA
Language: English Document Type: ARTICLE
Abstract: Metal-oxide-semiconductor capacitors in which the gate oxide has been replaced with a silicon rich **oxide** (SRO) **film** sandwiched between two thin **SiO2** layers are presented and investigated by transmission electron microscopy and electrical measurements. The grain size distribution and the amount of crystallized silicon remaining in SRO after annealing have been studied by transmission electron microscopy, whereas the charge trapping and the charge transport through the dots in the SRO layer have been extensively investigated by electrical measurements. Furthermore, a model, which explains the electrical behavior of such SRO capacitors, is presented and discussed.

23/3,AB/16 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07252641 Genuine Article#: 142BU Number of References: 31
Title: Read-disturb and endurance of SSI-Flash E(2)PROM devices at high operating temperatures (ABSTRACT AVAILABLE)
Author(s): DeBlauwe J (REPRINT) ; Wellekens D; Groeseneken G; Haspeslagh L; VanHoudt J; Deferm L; Maes HE
Corporate Source: LUCENT TECHNOL,/MURRAY HILL//NJ/07974 (REPRINT); IMEC,/B-3001 LOUVAIN//BELGIUM/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1998, V45, N12 (DEC), P 2466-2474

ISSN: 0018-9383 Publication date: 19981200
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: The high-temperature (T) reliability behavior of merged-transistor source side injection (SSI) **Flash** nonvolatile **memory** (NVM) devices is evaluated in terms of endurance and disturb effects related to stress induced leakage current (SILC), and correlated with the high-T behavior (generation, anneal) of oxide traps. As compared to room-T, program/erase (P/E) cycling at 150 degrees C results in an improved endurance due to an enhanced charge emission. The impact of the operating temperature on SILC-related disturb effects, on the other hand, depends on two combined effects in memory cells where large local charge trap-up influences the threshold voltage, V-t: 1) the T-enhanced trap generation and 2) the T-enhanced emission of trapped charge which influences the disturb field. In the case of the HIMOS-cell-which is discussed here-long-term nonvolatility can still be guaranteed at 150 degrees C.

Finally, bake tests at higher temperatures (250-300 degrees C) have been performed in order to evaluate the persistence of the generated damage, It is found that bulk oxide traps are not cured by the bake and, therefore, no long-term relief of SILC-related disturb effects is expected at 150 degrees C.

23/3,AB/17 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05730560 Genuine Article#: WU031 Number of References: 10
Title: A new ultra low voltage silicon-rich-oxide (SRO) NAND cell (ABSTRACT AVAILABLE)
Author(s): Lin CJ (REPRINT) ; Hsu CCH; Chen HH; Hong G
Corporate Source: NATL TSING HUA UNIV,DEPT ELECT ENGN, MICROELECT LAB, STAR GRP/HSINCHU 300//TAIWAN/ (REPRINT)
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1997, V36, N3A (MAR), P1030-1034
ISSN: 0021-4922 Publication date: 19970300
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: Thin silicon-rich-**oxide** (SRO) **film** can be an efficient and reliable tunneling injector for the low voltage application in **Flash memory** cell. To date, no work has been done on the quantitative and microscopical tunneling model for the SRO enhancement behavior. Moreover. no complete investigation on array-level SRO Flash cell have been presented. In this paper, a new low voltage SNAND (SRO NAND) cell is proposed and investigated, especially in term of performance characteristics and reliability issues, Furthermore, a two-dimensional microscopical model for SRO tunneling characteristics is developed to quantitatively explain the tunneling enhancement characteristics for SRO **Flash memory** cell. Results show that the tunneling model agrees well with the tunneling characteristics of SNAND cell and also provided the insight into tunnel oxide scaling in SNAND cell operation. The erase and program voltage can be reduced from 22 V to 7 V and 12 V with improved erase speed up to 2 orders, respectively. More than 10(5) endurance cycles are achieved. The feasibility of the SNAND cell is demonstrated.

12/06/2002

23/3,AB/18 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

05721925 Genuine Article#: WT457 Number of References: 12
Title: Impact of tunnel film oxynitridation on band-to-band tunneling current and electron injection in **flash memory** (ABSTRACT AVAILABLE)
Author(s): Arakawa T (REPRINT) ; Matsumoto R; Hayashi T
Corporate Source: OKI ELECT IND CO LTD,MICROSYST TECHNOL, 550-5 HIGHASHIASAKAWA/HACHIOJI/TOKYO 193/JAPAN/ (REPRINT); OKI ELECT IND CO LTD,VLSI RES & DEV CTR/HACHIOJI/TOKYO 193/JAPAN/; OKI ELECT IND CO LTD,LSI PROC TECHNOL DIV/HACHIOJI/TOKYO 193/JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1997, V36, N3B (MAR), P1351-1354
ISSN: 0021-4922 Publication date: 19970300
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: The impact of the use of oxynitride tunnel film on write, erase and read operations of **flash memories** was investigated. We found that during electron ejection from a floating gate into a drain, band-to-band tunneling currents of **flash memory** cells with tunnel films having a high degree of nitridation are two orders of magnitude smaller than that of **flash memory** cells with **oxide** tunnel **films**. Consequently, higher-nitridation tunnel films improve the endurance characteristics of **flash memory** . However, during electron injection from a channel into the floating gate, Fowler-Nordheim tunneling gate currents of **flash memory** cells with higher-nitridation tunnel films are two orders of magnitude smaller than that of **flash memory** cells with **oxide** tunnel **films**. Moreover, the threshold voltage of **flash memory** cells with oxynitride tunnel films is 0.24-0.48 V smaller than that of **flash memory** cells with **oxide** tunnel **films** in read operations. These results can be explained by the modification of the electric field under oxynitride tunnel films due to the formation of donor layers, which is induced by nitridation of tunnel **oxide films**.

23/3,AB/19 (Item 7 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

05024111 Genuine Article#: VA047 Number of References: 20
Title: ELECTRICAL AND RADIATION TESTS OF THIN TUNNEL OXIDES (Abstract Available)
Author(s): PACCAGNELLA A; RIZZATO A; SCARPA A; ZANONI E; CRISENZA G; GHIDINI G
Corporate Source: UNIV PADUA,DIPARTIMENTO ELETTRON & INFORMAT,VIAG GRADENIGO 6-A/I-35131 PADUA//ITALY/; SGS THOMSON MICROELECTR,CENT R&D/I-20041 AGRATEBRIANZA/MI/ITALY/
Journal: MICROELECTRONICS AND RELIABILITY, 1996, V36, N7-8 (JUL-AUG), P 1033-1044
ISSN: 0026-2714
Language: ENGLISH Document Type: ARTICLE
Abstract: The effects of constant current stress and Co-60 gamma irradiation on MOS capacitors with tunnel oxide have been investigated. The thin tunnel oxide is one of the topic steps of **Flash** EEPROM **memories** technological process. Two different device technologies have been used. We have observed a qualitative agreement between the

results obtained with the two methods, indicating that also radiation testing can be a valuable tool to investigate the quality of thin tunnel **oxide layers**. Copyright (C) 1996 Elsevier Science Ltd.

23/3,AB/20 (Item 8 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03965535 Genuine Article#: QV389 Number of References: 10
Title: BLOCK-ERASING METHODS FOR **FLASH MEMORY** (Abstract Available)
Author(s): SHIBA K; KUBOTA K
Corporate Source: HITACHI LTD,DIV SEMICOND & INTEGRATED CIRCUIT/KODAIRA/TOKYO 187/JAPAN/
Journal: ELECTRONICS AND COMMUNICATIONS IN JAPAN PART II-ELECTRONICS, 1994, V77, N4 (APR), P106-113
ISSN: 8756-663X
Language: ENGLISH Document Type: ARTICLE
Abstract: Methods for dividing **flash memory** arrays into erasable blocks of flexible size have been studied. Blocks are partitioned along the word lines and the **source** lines in different blocks are disconnected. A minimum block is formed along one word lines from which blocks different in volume are constituted easily. In this dividing scheme, the data disturb time of unselected blocks becomes longer, resulting in undesirable threshold reduction.

It was found that this data disturb endurance is improved by biasing the **source** at about 5 V. When the state is ''1,'' it prevents channel formation so that no hot hole injection into the floating gate takes place. In the case of ''0'' state, this bias reduces the electric fields between the floating gate and the **drain**; and hence the F-N tunneling current is suppressed. By this method, data disturb endurance in unselected blocks was improved to be more than 10,000 cycles.

23/3,AB/21 (Item 9 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03413696 Genuine Article#: PD538 Number of References: 0
(NO REFS KEYED)
Title: HIGHLY RELIABLE **FLASH MEMORIES** FABRICATED BY IN-SITU MULTIPLE RAPID THERMAL-PROCESSING (Abstract Available)
Author(s): HAYASHI T; KAWAZU Y; UCHIYAMA A; FUKUDA H
Corporate Source: OKI ELECT IND CO LTD,SEMICOND TECHNOL LAB,DEPT ULSI/HACHIOJI 193//JAPAN/
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1994, VE77C, N8 (AUG), P 1270-1278
ISSN: 0916-8524
Language: ENGLISH Document Type: ARTICLE
Abstract: We propose, for the first time, highly reliable flash-type EEPROM cell fabrication using in-situ multiple rapid thermal processing (RTP) technology. In this study, rapid thermal oxynitridation tunnel **oxide** (RTONO) **film** formations followed by in-situ arsenic (As)-doped floating-gate polysilicon growth by rapid thermal chemical vapor deposition (RTCVD) technologies are fully utilized. The results show that after 5 x 10(4) program/erase (P/E) endurance cycles, the conventional cell shows 65% narrowing of the threshold voltage (V(t))

window, whereas the RTONO cell indicates narrowing of less than 20%. A large number of nitrogen atoms (approximately-greater-than 10(20) atoms/cm3) are confirmed by secondary ion mass spectrometry (SIMS), pile up at the **SiO2**/Si interface and distribute into bulk **SiO2**. It is considered that in the RTONO film stable Si-N bonds are formed which minimize electron trap generation as well as the neutral defect density, resulting in lower V(t) shifts in P/E stress. In addition, the RTONO film reduces the number of hydrogen atoms because of final N2O oxynitridation. The SIMS data shows that by the in-situ RTCVD process As atoms (9 x 10(20) atoms/cm3) are incorporated uniformly into 1000-angstrom-thick film. Moreover, the RTCVD polysilicon film indicates an extremely flat surface. The time-dependent dielectric breakdown (TDDB) characteristics of interpoly **oxide**-nitride-**oxide** (ONO) **film** exhibited no defect-related breakdown and 5 times longer breakdown time as compared to phosphorus-doped polysilicon film. Therefore, the flash-EEPROM cell fabricated has good charge storing capability.

23/3,AB/22 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04955839 JICST ACCESSION NUMBER: 01A0700104 FILE SEGMENT: JICST-E
Analysis of Gate Disturbance Degradation by Nitridation of Flash Tunnel Oxide.
ARAI M (1); HASHIDZUME T (1); NITTA T (1); ODAKE Y (1); MATSUO I (1)
(1) Matsushita Electronics Corp., Kyoto, Jpn
Jpn J Appl Phys Part 1, 2001, VOL.40,NO.4B, PAGE.2969-2976, FIG.14, TBL.1, REF.26
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 621.382.08
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In this work, an experimental analysis of gate disturbance degradation with negative bias stress caused by nitridation of flash tunnel oxide has been performed. Nitrided tunnel oxlde successfully suppresses gate disturbance with positive bias stress, however, it enhances gate disturbance with negative bias stress. A slmilar gate polarity dependence has been observed in charge-to-breakdown and gate voltage shifts during Fowler-Nordheim stress. We propose the following dual-quality-layer model, which can explain all the polarity results. A poor-quality **layer** compared with base **oxide** is concurrently formed at the region where nitrogen atoms do not exist during nitridation. Subsequent to program/erase stress, more hole traps are created at the surface of tunnel oxide and modulate the energy band at the surface of tunnel oxide. Therefore, electrons can easily tunnel through the oxide with a negative bias stress because of the reduced barrier height at the surface of tunnel oxide. (author abst.)

23/3,AB/23 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04803048 JICST ACCESSION NUMBER: 96A0819089 FILE SEGMENT: JICST-E
The Effect of the Floating Gate/Tunnel **SiO2** Interface on **FLASH Memory** Data Retention Reliability.
MURAMATSU SATORU (1); ANDO KOICHI (1); KUBOTA TAISHI (1)

(1) NEC Corp.
Denshi Joho Tsushin Gakkai Taikai Koen Ronbunshu(Proceedings of the IEICE General Conference (Institute of Electronics, Information and Communication Engineers), 1996, VOL.1996,NO.Society C2, PAGE.261-262, FIG.9, REF.2
JOURNAL NUMBER: G0508AEP
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication

23/3,AB/24 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04729923 JICST ACCESSION NUMBER: 00A1024610 FILE SEGMENT: JICST-E
Research on Formation of Ultra-thin Gate Oxide by Using Water Vapor Generator(WVG).
NAKAMURA OSAMU (1)
(1) Tohoku Univ.
Tohoku Daigaku Dentsu Danwakai Kiroku(Record of Electrical and Communication Engineering Conversazione, Tohoku University), 2000, VOL.69,NO.1, PAGE.103-106, FIG.6
JOURNAL NUMBER: F0511AAU ISSN NO: 0385-7719
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: In nonvolatile **memories** such as **flash memory**, the thin **oxide film** is used as a tunneling dielectric for electron transportation to the floating gate in semiconductor manufacturing. The **oxide film** should have a strong dielectric strength the reason why electron tunneling is carried out under high electric field condition. During transportation of the carriers through the oxide, some of them are trapped in **oxide film**. Carrier trapping gives rise to the space charge in the oxide, causing window narrowing and oxide breakdown. Therefore, high-reliability ultra-thin oxide is required for nonvolatile memories. The purpose of this paper investigates performance of a newly developed WVG system by catalytic reaction for gate oxide formation process required ultraclean ambience. The dependence of electrical characteristics on gate oxidation ambience using WVG system was investigated. From these results, we suggest a newly developed technology for ultra-thin gate oxide formation with high reliability. (author abst.)

23/3,AB/25 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03399725 JICST ACCESSION NUMBER: 97A0823165 FILE SEGMENT: JICST-E
Nitrogen and Phosphorus co-doped Amorphous Silicon as a Floating Gate of **Flash Memory**.
KANEOKA T (1); ANMA M (1); ITOH H (1); OHNO Y (1); HIRAYAMA M (1)
(1) Mitsubishi Electric Corp., Hyogo, JPN
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners),

1997, VOL.97,NO.195(SDM97 43-67), PAGE.73-80, FIG.17, TBL.1, REF.3
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The impact of an in-situ nitrogen and phosphorus co-doped amorphous silicon as a scalable floating gate material for future **flash memories** is discussed. An oxidation-resistant surface with a homogeneous and smooth texture of the crystallized in-situ nitrogen and phosphorus co-doped amorphous silicon improves the reliability of the interpolyCVD-**SiO2** dielectric remarkably. The tunnel oxide at the edge of the floating gate is immune from the loss of the reliability because little loss of the gate dimension, achieved by the oxidation-resistant feature, secures an enough floating gate area overlapping with the source as designed. The in-situ nitrogen and phosphorus co-doped a-Si is a promising floating gate material that can well function in the scaled-down **flash memory**. (author abst.)

23/3,AB/26 (Item 5 from file: 94)

03241193 JICST ACCESSION NUMBER: 98A0027520 FILE SEGMENT: PreJICST-E
Reduction of Electron Traps in CVD **SiO2** Single **Layer** Interpoly **Dielectric films** for **Flash Memories**.
KATAYAMA ATSUKO (1); KOBAYASHI TAKASHI (1); KUME HITOSHI (1); KIMURA KATSUTAKA (1)
(1) Hitachi, Ltd., Cent. Res. Lab.
Oyo Butsuri Gakkai Gakujutsu Koenkai Koen Yokoshu, 1997, VOL.58th,NO.2, PAGE.802
JOURNAL NUMBER: Y0055AAA
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
MEDIA TYPE: Printed Publication

23/3,AB/27 (Item 6 from file: 94)

02782021 JICST ACCESSION NUMBER: 96A0569422 FILE SEGMENT: JICST-E
Tunnel Oxide Reliability Improvement by Si/**SiO2** Interface Strain Relaxation with Rapid Thermal, High Temperatures Steam Oxidation.
TOMITA HIROSHI (1); OZAWA YOSHIO (1); TAKAHASHI MAMORU (2)
(1) Toshiba Purosesugiken; (2) Toshiba Kankyogiken
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1996, VOL.96,NO.63(SDM96 16-25), PAGE.1-8, FIG.14, TBL.2, REF.7
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 539.23:54-31 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Simultaneous improvement of tunnel oxide reliability, such as stress-induced leakage current, hole trap, electron trap and charge-to-breakdown (Qbd) characteristics, has been desired to achieve

high performance of **Flash Memories**. In this paper, we propose a novel RTO(rapid thermal oxidation) process to realize excellent tunnel oxide characteristics for the first time. Essence of the process is combination with rapid thermal, high temperature and diluted steam oxidation processes. As the results of O1s peak observations by X-ray Photoelectron Spectroscopy(XPS), mechanism of reliability improvement compared to the traditional steam oxidation process is expected to reduce weak Si-O bonds and/or imperfections of Si-O network near Si/**SiO2** interface by viscous relaxation. (author abst.)

23/3,AB/28 (Item 7 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02741497 JICST ACCESSION NUMBER: 96A0414736 FILE SEGMENT: JICST-E
Technology for Fabricating Highly Reliable Tunnel **Oxide Films**.
TERAMOTO AKINOBU (1); MATSUI YASUJI (1); KOBAYASHI KIYOTERU (1); UMEDA HIROSHI (1); NAKAMURA TADASHI (2)
(1) Mitsubishi Electric Corp.; (2) Mitsubishisemikondakutashisutemuenjiniaringu
Mitsubishi Denki Giho, 1996, VOL.70,NO.3, PAGE.317-321, FIG.10, REF.5
JOURNAL NUMBER: F0198AAP ISSN NO: 0369-2302 CODEN: MTDNA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The write cycle lifetime of a **flash memory** device is limited by the reliability of the **SiO2** tunnel film, whose failure modes include dielectric breakdown, electron capture and excess currents. The authors investigated the relation beween **dielectric** breakdown, **film** thickness and film area. They also determined that injected holes in the **oxide layer** are responsible for excess currents. Nitriding the **oxide layer** was found effective for suppressing electron capture and excess currents. (author abst.)

23/3,AB/29 (Item 8 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02713152 JICST ACCESSION NUMBER: 95A0942247 FILE SEGMENT: JICST-E
VLSI technology. 19. Device and process. Part 9. The reliability of **oxide film** necessary for nonvolatile semiconductor memory.

MASUOKA FUJIO (1)
(1) Toshiba Corp., ULSI Res. Cent.
Handotai Kenkyu, 1995, VOL.41, PAGE.29-64, FIG.60, TBL.2, REF.104
JOURNAL NUMBER: X0816AAU
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: To materialize a highly reliable **flash memory**, operation of the **flash memory**, and structure and a manufacture method for an **oxide film** are discussed. At first, operation principles of writing and erasure of various

flash memories are described. Secondarily, degradation of the **oxide film** caused by charge injection to the **oxide film** or a manufacture method of a thin **oxide film** are examined respectively by using Si rich **SiO2** .Lastly, degradation caused by difference in operation principles is examined by comparing a **flash memory** using a overall bipolarity FN tunnel diode for write and erasure, with other memories.

23/3,AB/30 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02707749 JICST ACCESSION NUMBER: 96A0203842 FILE SEGMENT: JICST-E
Formation of ultrathin **oxide films**.
IWAMOTO TOSHIYUKI (1); MIYAKE TOSHINORI (1); OMI TADAHIRO (1)
(1) Tohoku Univ., Fac. of Eng.
Busseiken Dayori, 1996, VOL.35,NO.5, PAGE.41-46, FIG.10, TBL.1, REF.4
JOURNAL NUMBER: F0457AAT ISSN NO: 0385-9843
UNIVERSAL DECIMAL CLASSIFICATION: 539.23:54-31 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

23/3,AB/31 (Item 10 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02333224 JICST ACCESSION NUMBER: 95A0451252 FILE SEGMENT: JICST-E
The Effect on the Tunnel **Oxide** Characteristics of **Insulator Films** on the Gate Electrode.
USHIYAMA MASAHIRO (1); YASHIMA HIDEYUKI (1); KUME HITOSHI (1); MIURA HIDEO (2); ADACHI TETSUO (3); NISHIMOTO TOSHIAKI (3); KOMORI KAZUHIRO (3); KATO MASATAKA (3); OJI YUZURU (3)
(1) Hitachi, Ltd., Cent. Res. Lab.; (2) Hitachi, Ltd., Mech. Eng. Res. Lab.; (3) Hitachi, Ltd.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.10(SDM95 6-18), PAGE.27-33, FIG.10, REF.3
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS 621.382.08
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We have investigated the effect on the tunnel **oxide** characteristics of **insulator films** on the gate electrode. Electron traps are generated in tunnel oxides by high-temperature oxidation of a Si3N4 film in an ONO film on the gate electrode. Microscopic Raman spectroscopy and wafer bending showed that the oxidation of the Si3N4 film generates stronger tensile stress in the poly-Si gate electrode. The stress is thought to weaken the bonds of tunnel oxides, which may generate electron traps. (author abst.)

23/3,AB/32 (Item 11 from file: 94)
DIALOG(R)File 94:JICST-EPlus

12/06/2002

01765899 JICST ACCESSION NUMBER: 93A0547293 FILE SEGMENT: JICST-E
High-Performance Scaled Flash-Type EEPROMs with Heavily Oxynitrided Tunnel **Oxide Films**.
FUKUDA HISASHI (1); IWATANI MASAAKI (2); TSUJIMOTO MASAO (2); ONO TAKASHI (2); UCHIYAMA AKIRA (2)
(1) Oki Electric Industry Co., Ltd., Semiconductor Technology Lab.; (2) Oki Electric Industry Co., Ltd.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1993, VOL.93,NO.76(ICD93 24-33), PAGE.21-26, FIG.7, TBL.2, REF.9
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We have proposed a heavy oxynitridation(RTONO) technology of the tunnel oxide, and successfully applied it to the scaled flash-type EEPROMs. Excellent program and erase(P/E) endurance properties were obtained with much small window closure (less than 6%). In addition, good P/E speeds are also obtained. The SIMS results show that a large number of N atoms (>1020 atoms/cm3) are incorporated into **SiO2**, while the number of H atoms is decreased. Accordingly, almost no increase of trapped charge by the P/E stress is induced. Thus, this technology is the key to providing flash-EEPROM in the submicron regime. (author abst.)

23/3,AB/33 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1166369 H.W. WILSON RECORD NUMBER: BAST94034961
Effect of oxidation ambient on the dielectric breakdown characteristics of thermal **oxide films** of silicon
Murakami, Yoshio; Shiota, Takaaki; Shingyouji, Takayuki
Journal of Applied Physics v. 75 pt1 (May 15 '94) p. 5302-5
DOCUMENT TYPE: Feature Article ISSN: 0021-8979

ABSTRACT: The dielectric breakdown characteristics of thermal **oxide films** grown by dry and wet oxidation are investigated. The reliability of gate oxide is a very important problem in such MOS devices as dynamic **RAM** and **flash memory**. It is found that the **oxide films** grown by wet oxidation have lower B-mode failure rates and greater B-mode breakdown fields than the **oxide films** grown by dry oxidation. In contrast, it is found that the reliability of the C mode of the **oxide films** does not differ consistently between the films grown by dry and wet oxidation. It is concluded from the results that as-grown defect causing B-mode failure may shrink or be reduced during wet oxidation.

23/3,AB/34 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14323667 PASCAL No.: 99-0531754
Proceedings of the 11th biennial conference on **Insulating Films** on Semiconductors, June 16-19, 1999, Kloster Banz, Germany
SCHULZ Max, ed; BRENDEL Rolf, ed
University of Erlangen, Institute of Applied Physics, Staudtstr. 7, 91058

Erlangen, Germany
University of Erlangen-Nuernberg, Germany.
INFOS'99 Biennial Conference on Insulating Films on Semiconductors, 11 (Kloster Banz DEU) 1999-06-16
Journal: Microelectronic engineering, 1999, 48 (1-4) 461 p.
Language: English

23/3,AB/35 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14111463 PASCAL No.: 99-0306592
Limitation current in Si SUB 3 N SUB 4 /SiO SUB 2 stacked **dielectric films**
TANAKA H
LSI Production Division, Oki Electric Industry, 550-Higashi-Asakawa, Hachioji, Tokyo 193-8550, Japan
Journal: Applied surface science, 1999, 147 (1-4) 222-227
Language: English
The limitation current in Si SUB 3 N SUB 4 /SiO SUB 2 stacked **dielectric films** has been investigated systematically for both field directions by using n SUP + and p SUP + polycrystalline Si (poly-Si) gate capacitors and by varying the bottom oxide thickness. It can be explained by the combination of Poole-Frenkel current in nitride layer and Fowler-Nordheim current in bottom **oxide layer** for all the cases. The trap depth for Poole-Frenkel current, the thickness of bottom oxide for Fowler-Nordheim current, and the barrier heights at the interfaces are the factors to determine the limitation current. The trap depths of holes and electrons for Poole-Frenkel current in nitride layer are calculated to be 0.6 and 0.9 eV, respectively. The limitation current with negative gate bias is thought to be Poole-Frenkel of holes and electrons both in nitride layer for thin (<= SUB >= 30 A) and thick (> 30 A) bottom oxides, respectively. On the other hand, the limitation current with positive gate bias is thought to be Poole-Frenkel of holes in nitride layer and Fowler-Nordheim of electrons in bottom **oxide layer** for thin and thick bottom oxides, respectively.

23/3,AB/36 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

14063997 PASCAL No.: 99-0255527
Properties of stacked **dielectric films** composed of SiO SUB 2 /Si SUB 3 N SUB 4 /SiO SUB 2
Proceedings of the 2nd Franco-Italian Symposium on SiO SUB 2 and Advanced Dielectrics
SANTUCCI S; LOZZI L; PASSACANTANDO M; PHANI A R; PALUMBO E; BRACCHITTA G; DE TOMMASIS R; TORSI A; ALFONSETTI R; MOCCIA G
SPINOLO G, ed; VEDDA A, ed; AUTRAN J L, ed; DEVINE R A B, ed
Dipartimento di Fisica and Unita INFM, Universita dell'Aquila, Via Vetoio 10 Coppito, 67010 L'Aquila, Italy; Texas Instruments Italia, Via Pacinotti 10, Avezzano (AQ), Italy
Dipartimento di Scienza dei Materiali, Universita degli Studi di Milano, Milan, Italy; Laboratoire de Physique de la Matiere, Institut National des Sciences Appliquees (INSA), Villeurbanne, France; France Telecom, CNET,

Meylan, France
French-Italian Symposium on SiO SUB 2 and Advanced Dielectrics, 2 (L'Aquila ITA) 1998-06-15
Journal: Journal of non-crystalline solids, 1999, 245 224-231
Language: English

Dielectric films composed of silicon **oxide** -nitride-oxide (ONO) structure have been grown over a polycrystalline silicon phosphorous-doped substrate. The films with a total thickness of about 30 nm have been obtained by two different deposition techniques of the top-**oxide layer** i.e. thermal oxidation of the nitride layers and low pressure chemical vapour deposition, while the bottom **oxide** and the nitride **layer** were obtained by thermal oxidation and low pressure chemical vapour deposition, respectively. The chemical composition was measured by XPS Auger parameter technique while the thickness of the deposited layers was determined by the X-ray reflectivity method and compared with the measurements performed on transmission electron microscopy cross-section images. The influence of the layer composition and thickness on the electrical properties of the whole **film**, used as **dielectric layer** of a capacitor with doped polycrystalline silicon as electrodes, have been investigated by measuring current as a function of voltage to study the mechanisms which contribute to an increase of the leakage current with increasing applied voltage. Furthermore, electrical erasable programmable read-only **flash memory** devices built using these **dielectric layers** in the floating gate structure have been measured for 'data retention loss' after thermal stress. The results give a complete picture on the role of the two topmost layers of the ONO structure towards the electrical behaviour.

23/3,AB/37 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

13338519 PASCAL No.: 98-0064909
Protonic nonvolatile field effect transistor memories in Si/SiO SUB 2 /Si structures
WARREN W L; FLEETWOOD D M; SCHWANK J R; SHANEYFELT M R; DRAPER B L; WINOKUR P S; KNOLL M G; VANHEUSDEN K; DEVINE R A B; ARCHER L B; WALLACE R M
Sandia Natl Lab, Albuquerque NM, United States
Proceedings of the 1997 IEEE Nuclear and Space Radiation Effects Conference, NSREC. Part 1 (of 3) (Snowmass Village, CO, USA) 1997-07-21/1997-07-25
Journal: IEEE Transactions on Nuclear Science, 1997, 44 (6 1) 1789-1798
Language: English

A low-voltage, radiation-tolerant, nonvolatile field effect transistor (NVFET) memory involving proton motion in SiO SUB 2 is illustrated in both bulk Si and silicon-on-insulator devices. We discuss a mechanism by which the protons are created in the **oxide layer** by a forming gas anneal. At low temperature (T<250 Degree C), the H SUP & plus; is largely imprisoned' in the buried SiO SUB 2 layer; i.e., the ions are sandwiched between the two encapsulating Si layers. The Si layers can be either c-Si or poly-Si, thus the technology is compatible with standard Si processing. The protons can be reliably and controllably drifted from one interface to another without any noticeable degradation in the signal past 10 SUP 6 cycles. Under an unbiased condition, the net proton density is not significantly affected by radiation up to at least 100 krad (SiO SUB 2). Last, we compare many of the properties of the NVFET to commercial **flash** nonvolatile **memories**.

23/3,AB/38 (Item 5 from file: 144)
DIALOG(R)File 144:Pascal

12274674 PASCAL No.: 95-0505025
Analyse et caracterisation des mecanismes de perte de charge relatifs aux dielectriques multicouches du point memoire EPROM
(Analyse and characterisation of charge loss mechanisms related to EPROM memory cell multilayer dielectric)
MAZOYER Pascale; MONDON F, dir
Universite de Grenoble 1, Saint-Martin-d'Heres, Francee
Univ.: Universite de Grenoble 1. Saint-Martin-d'Heres. FRA Degree: Th. doct.
1994-01; 1994 186 p.
Language: French Summary Language: French; English
L'evolution des memoires a semiconducteurs et en particulier de la famille EPROM (Erasable Read Only Memory) est liee a l'identification des phenomenes determinants du processus de perte de la charge electronique stockee. Les cellules etudiees ici sont toutes proches des points de fonctionnement de filieres industrialisees ou en cours de developpement (de 4 a 256 Megabits). On distingue deux mecanismes de perte de charge. Le premier est une fonction de la nature des dielectriques presents dans la structure et des lois qui regissent la conduction qui leur est associee. Le second est lie a la migration des ions alcalins dans la cellule. Partant de l'analyse des proprietes de la tricouche ONO (Oxyde Nitrure Oxyde) et en emettant l'hypothese de l'injection d'electrons en fin d'ecriture, un modele de perte de charge est propose. Il est base sur l'emission electronique assistee en temperature et la migration des electrons a travers l'ONO. Les mesures de perte de charge montrent qu'il ne faut pas descendre, dans la realisation de l'ONO, en deca de l'epaisseur tunnel de chaque couche et que l'obtention de couche d'epaisseur homogene et stoechiometrique ameliore la fiabilite du dispositif. Cette analyse conduit, de meme, a la proposition d'un dielectrique adapte aux applications tres avancees. Forme par l'association de nitrure et d'oxyde, le NO apparait comme un candidat interessant les generations EPROM et Flash EPROM 256 Mb. L'etude des contaminants ioniques a mis en oeuvre la methode TVS, qui s'avere un outil puissant, permettant l'evaluation rapide et precise de la densite d'ions mobile dans les dielectriques epais. Une solution economiquement viable a ete mise au point pour prevenir les effets d'une eventuelle contamination sur le plan memoire. Il s'agit de la juxtaposition judicieuse d'un verre au phosphore et d'un verre au bore et au phosphore

23/3,AB/39 (Item 6 from file: 144)
DIALOG(R)File 144:Pascal

12050209 PASCAL No.: 95-0246307
Relationship between nitrogen profile and reliability of heavely oxynitrided tunnel **oxide films** for flash electrically erasable and programmable ROMs
Solid state devices and materials
ARAKAWA T; HAYASHI T; OHNO M; MATSUMOTO R; UCHIYAMA A; JUKUDA H
TARUCHA SEIGO, ed; ARAKAWA YASUHIKO, ed; FUKUMA MASAO, ed; FURUYA KAZUHITO, ed; HORIKOSHI YOSHIJI, ed; IMAI HAJIME, ed; ISHIWARA HIROSHI, ed; KARAYAMA YOSHIFUMI, ed; MIYAO MASANOBU, ed; NAKASHIMA HISAO, ed; SHIRAKI YASUHIRO, ed; SUSAKI WATARU, ed; YOSHIMI MAKOTO, ed
Oki Electric Industry Co. Ltd, LSI Process technology div., Hachioji Tokyo 193, Japan

12/06/2002

Japan Society of Applied Physics, Tokyo, Japan.
SSDM'94. International conference (Yokohama, Kanagawa JPN) 1994-08-23
Journal: Japanese journal of applied physics, 1995, 34 (2B p.1) 1007-1011
Language: English

A larger charge-to-breakdown value and much less threshold-voltage narrowing in the endurance properties of flash electrically erasable and programmable ROMs were achieved by incorporating a greater amount of nitrogen (similar 10 SUP 2 SUP 1 atoms/cm SUP 3) into the bulk of thin **oxide films**, as well as near the oxide/Si interface. The charge to breakdown value of thin **oxide films** formed under an optimized heavy oxynitride condition (dry oxidation at 1100 Degree C; NH SUB 3 annealing at 1000 Degree C for 30 s; N SUB 2 O annealing at 1100 Degree C for 30 s) was four times as large as that of a conventional dry **oxide film**. These results were attributed to the suppression of stress-induced charge traps and the interface state, due to the introduction of nitrogen atoms in the oxide bulk, as well as at the oxide/Si interface

24/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7196408 INSPEC Abstract Number: A2002-07-4265K-081, B2002-04-4340K-053
Title: Second-harmonic generation from silicon nanocrystals embedded in SiO/sub 2/
Author(s): Jiang, Y.; Wilson, P.T.; Downer, M.C.; White, C.W.; Withrow, S.P.
Author Affiliation: Dept. of Phys., Texas Univ., Austin, TX, USA
Conference Title: Technical Digest. Summaries of papers presented at the Conference on Lasers and Electro-Optics. Postconference Technical Digest (IEEE Cat. No.01CH37170) p.552-3
Publisher: Opt. Soc. America, Washington, DC, USA
Publication Date: 2001 Country of Publication: USA 604+72 post deadline papers pp.
ISBN: 1 55752 662 1 Material Identity Number: XX-2001-01869
Conference Title: CLEO 2001. Technical Digest. Summaries of papers presented at the Conference on Lasers and Electro-Optics. Postconference Technical Digest
Conference Sponsor: IEEE/Lasers & Electro-Opt. Soc.; OSA-Opt. Soc. America; Quantum Electron. Division of the Eur. Phys. Soc.; Opt. Soc. Japanese Quantum Electron. Joint Group
Conference Date: 6-11 May 2001 Conference Location: Baltimore, MD, USA
Language: English
Abstract: Summary form only given. Si nanocrystals (ncs) embedded in SiO/sub 2/ are an essential ingredient of a new class of **flash memory** devices, and show promise as a nonlinear optical material for photonic device applications. We report an optical second-harmonic generation (SHG) study of nc-Si/SiO/sub 2/ nanocomposites. The results show that SHG from nc-Si/SiO/sub 2/ is sensitive to Si/SiO/sub 2/ electronic interface states and to electrostatic charging of the Si ncs, both essential features in their role in electronic device operation. SHG is also sensitive to transverse gradients in nc density, an essential feature in the design of photonic structures. Thus SHG uniquely characterizes materials and devices based on nc-Si/SiO/sub 2/.
Subfile: A B

24/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6880857 INSPEC Abstract Number: B2001-05-1265D-016
Title: Anomalous low temperature charge leakage mechanism in ULSI **flash memories**
Author(s): Lam, C.; Sunaga, T.; Igarashi, Y.; Ichinose, M.; Kitamura, K.; Willets, C.; Johnson, J.; Mittl, S.; White, F.; Tang, H.; Chen, T.-C.
Author Affiliation: Microelectron. Div., IBM Corp., Hopewell Junction, NY, USA
Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.335-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 871 pp.
ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191
U.S. Copyright Clearance Center Code: 0 7803 6438 4/2000/$10.00
Conference Title: International Electron Devices Meeting. Technical Digest. IEDM
Conference Sponsor: Electron Devices Soc. IEEE

Conference Date: 10-13 Dec. 2000 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We present a systematic study of an anomalous charge leakage phenomenon in **flash memories** which occurs at temperatures below 150 degrees C. Essential characteristics of the leakage are described in association with various process parameters. A new leakage mechanism based on diffusion of an ionic entity produced by regenerative electrochemical reactions through percolating networks in the **silicon dioxide** is proposed.
Subfile: B

24/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6403703 INSPEC Abstract Number: B1999-12-1265D-021
Title: Hole trapping due to anode hole injection in thin tunnel gate oxides in memory devices under Fowler-Nordheim stress
Author(s): Samanta, P.
Author Affiliation: Dept. of Phys., Jadavpur Univ., Calcutta, India
Journal: Applied Physics Letters vol.75, no.19 p.2966-8
Publisher: AIP,
Publication Date: 8 Nov. 1999 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19991108)75:19L.2966:HTAH;1-P
Material Identity Number: A135-1999-044
U.S. Copyright Clearance Center Code: 0003-6951/99/75(19)/2966(3)/$15.00
Language: English
Abstract: Hole trapping characteristics in thin (10 nm) thermally grown **silicon dioxide** (SiO/sub 2/) in **flash memory** device with n-type floating polycrystalline silicon (poly-Si) gate have been theoretically investigated under Fowler-Nordheim (FN) constant current and voltage stress. Theoretical results of gate voltage shift Delta V/sub G/ or Delta V/sub FN/ due to trapped holes show good agreement with experimental data of Park and Schroder [IEEE Trans. Electron Devices ED-45, 1361 (1998)] during constant current injection. Our theoretical analysis based on hole injection from the poly-Si gate (anode) at injected electron fluence Q/sub inj/ as low as 0.01 C/cm/sup 2/ address that constant voltage stress degrades the gate oxide quality faster than constant current stress due to enhanced charge trapping and trap creation rate under constant voltage stress.
Subfile: B

24/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4499308 INSPEC Abstract Number: A9322-7340Q-002
Title: Ion beam mixing for enhanced electron tunneling in metal-oxide-silicon structures
Author(s): Walker, A.J.; Politiek, J.
Author Affiliation: Philips Res. Lab., Eindhoven, Netherlands
Journal: Applied Physics Letters vol.63, no.6 p.758-60
Publication Date: 9 Aug. 1993 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/93/63(6)/758/3/$6.00

Language: English
Abstract: Metal-oxide-silicon (MOS) structures were fabricated to investigate enhanced Fowler-Nordheim tunneling in thin oxides due to ion beam mixing. Ions of germanium were implanted into a 100 nm polycrystalline silicon layer deposited on 10 nm thermal **silicon dioxide** such that the tail of the implant profile contains the thin oxide. Besides simple MOS capacitors and transistors, flash electrically erasable programmable read only **memory** (**flash** EEPROM) cells were fabricated for the first time using this technique. Using 1*10/sup 15/ cm/sup -2/ at 80 keV the Fowler-Nordheim tunneling barrier reduced by about 0.9 eV at the polycrystalline gate/oxide interface and by 1.3 eV at the oxide/substrate interface. The consequently lower program/erase voltages in the flash EEPROM were measured. Flash EEPROM charge retention measurements show that the discharge process is logarithmic in time. This leads to the possibility of flash EEPROMs being programmed and erased at low voltages and having sufficient charge retention for several years operation.
Subfile: A

24/3,AB/5 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1976804 NTIS Accession Number: PB96-212659
Sharp Technical Journal, Volume 61, April 1995
Sharp Corp., Nara (Japan).
Corp. Source Codes: 090131000
cApr 95 83p
Languages: Japanese
Journal Announcement: GRAI9624
Text in Japanesee with English abstracts. Portions of this document are not fully legible. See also PB96-212642 and PB96-212634.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC E08/MF E08
Contents: Present Situation and Trend of Electronic Packaging Technology; Thermal Stabilization Technique of Power HBTs; A Low Noise Fan Operating in Inlet Distortions; Development of 2.4 GHz Low Power Data Communication System; An Automatic Protocol Recognition Scheme of Infrared Communication Protocols; Development of a Three Dimensional Illuminance Analysis System Using Ray Tracing Method; Reliable Red-Emitting Laser Diodes Grown by Solid-Source Molecular Beam Epitaxy; Low Temperature Deposition of High Quality **Silicon Dioxide** Films; Switching Power Supply Simulation by PSpice; Development of MD-DATA Drive Unit; Development of Rehabilitation Software for Cognitive Function Retarded Patients; 'Azayaka Shoin' Japanese Color Word Processor WD-C700; Automatic Washing Machine with Economized Water Mechanism ES-S65; Vacuum Cleaner with Edge Clean Function; 5V Only 16M/8M **Flash Memory**; Primary Regulator for Power Supply.

24/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06128550
E.I. No: EIP02377079425
Title: Impact of floating gate dry etching on erase characteristics in NOR **flash memory**

Author: Lee, Wook H.; Lee, Dong-Kyu; Na, Young-Ho; Kim, Keon-Soo; Ahn, Kun-Ok; Suh, Kang-Deog; Roh, Yonghan
Corporate Source: NVM Team Memory Division Samsung Electronics, Ltd., Yong-In 449-711, South Korea
Source: IEEE Electron Device Letters v 23 n 8 August 2002. p 476-478
Publication Year: 2002
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: We report the effects of plasma process-induced damage during floating gate (FG) dry-etching process on the erase characteristics of NOR flash cells. As compared to flash cells processed in a stable plasma condition, it is found that flash cells processed in the nonoptimized ambient show significantly degraded erase characteristics under a negative gate Fowler-Nordheim (FIN) bias, exhibiting a fast-erasing bit in the distribution of erased bits. However, little differences are found in their tunneling characteristics under a positive gate biasing. The gate bias polarity dependence of FN tunneling indicates that positive charges are created near the poly-Si/SiO//2 interface during the FG dry-etching, prior to the backend processes such as metal- or via-etch. 10 Refs.

24/3,AB/7 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06072315
E.I. No: EIP02256984681
Title: Concept of floating-dot memory transistors on silicon-on-insulator substrate
Author: Winkler, O.; Merget, F.; Heuser, M.; Hadam, B.; Baus, M.; Spangenberg, B.; Kurz, H.
Corporate Source: Institut fur Halbleitertechnik RWTH Aachen, 52074 Aachen, Germany
Conference Title: Micro and Nano Engineering 2001
Conference Location: Grenoble, France Conference Date: 20010916-20010919
E.I. Conference No.: 59160
Source: Microelectronic Engineering v 61-62 July 2002. p 497-503
Publication Year: 2002
CODEN: MIENEF ISSN: 0167-9317
Language: English
Abstract: The concept of floating dot transistors on silicon-on-insulator substrate was discussed. With the concept of nanodots in **silica** environments an architecture where oxidized floating nanodots were embedded directly in a gate material was also investigated. The principle of flashing memories is storing electric-charge on non-contacted, floating gates. This charge can influence the switching behavior of a MOS field-effect-transistors (MOSFET). The charge of the nanodots was controlled by the applied voltage of the transistor gate electrode. (Edited abstract) 7 Refs.

24/3,AB/8 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06015543
E.I. No: EIP02106878523
Title: Coupled Si and SiO//2 Monte Carlo device simulator for accurate gate current calculation
Author: Ezaki, Tatsuya; Nakasato, Hiroki; Hane, Masami

Corporate Source: Silicon Systems Res. Laboratories NEC Corporation, Sagamihara, 229-1198, Japan
Conference Title: IEEE International Electron Devices Meeting IEDM 2001
Conference Location: Washington, DC, United States Conference Date: 20011202-20011205
E.I. Conference No.: 59030
Source: Technical Digest - International Electron Devices Meeting 2001. p 485-488 (IEEE cat n 01CH37224)
Publication Year: 2001
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A new MOSFET device simulator has been developed based on a coupled Monte Carlo procedure for the carrier transport in both Si and SiO//2 regions. This simulator accounts for the image-force effect that modulates potential barrier height for the electron injected into SiO//2. Gate currents are calculated combining both the hot carrier injection and the back-scattering from the SiO//2 region arising from the potential modulation. **Flash memory** cell simulations were performed by this method. The actual MOSFET gate currents and the programming characteristics of the **flash memory** cells could be reproduced quantitatively without using any adjustable parameters. 4 Refs.

24/3,AB/9 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05937493
E.I. No: EIP01466728294
Title: Electrical degradation and recovery of dielectrics in n**+**+-poly-Si/SiO//x/SiO//2/p-sub structures designed for application in low-voltage non-volatile memories
Author: Irrera, F.
Corporate Source: Department of Electronics University of Rome La Sapienza, I-00184 Rome, Italy
Source: Microelectronics Reliability v 41 n 11 November 2001. p 1809-1813
Publication Year: 2001
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: In this paper we study the degradation and recovery of dielectrics in n**+**+-poly-Si/SiO//x/SiO//2/p-sub capacitors designed for application in low-voltage **flash** EEPROM **memories**. Constant current stress experiment have been performed and the gate voltage in the Fowler-Nordheim (FN) regime and the flat-band voltage monitored. Experiment demonstrated that SiO//x has a greater tendency to trap electrons than pure SiO//2 and exhibits a larger voltage shift in the FN regime after electrical stress. On the other hand, permanent recovery of the leakage current can be obtained by injection of current at very low flux. This effect has been tentatively explained with the annealing of native metastable defects occurring in concurrence with the stress induced creation of new traps. copy 2001 Elsevier Science Ltd. All rights reserved. 6 Refs.

24/3,AB/10 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05550238
E.I. No: EIP00055162451
Title: Bake induced charge gain in NOR flash cells

Author: Fastow, R.; Ahmed, K.; Haddad, S.; Randolph, M.; Huster, C.; Hom, P.
Corporate Source: Advanced Micro Devices, Sunnyvale, CA, USA
Source: IEEE Electron Device Letters v 21 n 4 2000. p 184-186
Publication Year: 2000
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: Charge gain, caused by localized defects in the tunnel oxide of floating gate devices, is one of the central reliability concerns of **flash memory**. In this letter, we show that charge motion in the poly sidewall spacers of flash cells can also result in substantial charge gain, for nonoptimized processes. Data showing the time, temperature, and field dependencies of this charge gain mechanism are presented. It is shown that the threshold voltage shift caused by charge motion in the poly sidewall spacers follows the simple factorial expression: Delta V//t//h equals C center dot V//f//g center dot t** alpha center dot e** minus ** epsilon **a**/**k**T. (Author abstract) 12 Refs.

24/3,AB/11 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05498159
E.I. No: EIP00025058103
Title: Nonvolatile, high density, high performance phase change memory
Author: Wicker, Guy
Corporate Source: Ovonyx, Inc, Troy, MI, USA
Conference Title: Proceedings of the 1999 Design, Characterization, and Packaging for MEMS and Microelectronics
Conference Location: Royal Pines Resort, Aust Conference Date: 19991027-19991029
E.I. Conference No.: 56257
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3893 1999. p 2-9
Publication Year: 1999
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: A nonvolatile memory that is potentially denser, faster, and easier to make than DRAM is developed. It relies on phase transitions by nanosecond heating and cooling of small regions of the memory cell. Initial target markets are **flash memory**, embedded **memory** and DRAM. 19 Refs.

24/3,AB/12 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05460344
E.I. No: EIP00014972390
Title: MeV implantation introduced damage at the LOCOS bird's beak in 0.35 mu m **Flash Memory** devices
Author: Wu, Hong J.; Bhattacharya, Surya; Krishnamurthy, Shyam; Sharma, Umesh
Corporate Source: Rockwell Semiconductor Systems, Newport Beach, CA, USA
Conference Title: Proceedings of the 1998 International Conference on 'Ion Implantation Technology' Proceedings (IIT'98)
Conference Location: Kyoto, Jpn Conference Date: 19980622-19980626
E.I. Conference No.: 56231
Source: Proceedings of the International Conference on Ion Implantation

Technology v 2 1999. IEEE, Piscataway, NJ, USA. p 937-938
Publication Year: 1999
CODEN: 002596 ISBN: 0-7803-4538-X
Language: English
Abstract: This paper reports on the impact of high energy (MeV) retrograde well implants on the reliability of **Flash Memory** devices. These implants are shown to severely damage the oxide at the LOCOS bird's beak edge. The degree of SiO//2 amorphization caused by the high-energy ion implantation is shown to be enhanced by the LOCOS structure. The amorphization causes accelerated oxide loss during subsequent oxide etch-backs. Both performance and reliability of **Flash Memory** cells is degraded due to this damage. We demonstrate a technique for reducing the implant induced damage and thereby improve device performance and reliability. (Author abstract) 2 Refs.

24/3,AB/13 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05020479
E.I. No: EIP98054209256
Title: Breakdown of reoxidized nitrided oxide (ONO) in **Flash memory** devices upon current stressing
Author: Cha, C.L.; Chor, E.F.; Gong, H.; Zhang, A.Q.; Chan, L.
Corporate Source: Natl Univ of Singapore, Singapore, Singapore
Conference Title: Proceedings of the 1997 IEEE Hong Kong Electron Devices Meeting
Conference Location: Hong Kong, Hong Kong Conference Date: 19970830
E.I. Conference No.: 48336
Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA. p 82-85
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: The characteristic of reoxidized nitrided SiO//2 (ONO) breakdown in **Flash memory** devices, upon current stressing is being investigated. Results indicate that current stressing on the ONO layer is very detrimental to the performance of the Flash device, and this situation is inevitable during the device fabrication. It is found that with a constant current of 5 mu A passing through an ONO layer of `200A' thickness (with an area of 50,000 mu m**2), it takes just only a mere 20 seconds to kill the device. The situation worsens when the polarity is reversed (a negative current of the same magnitude passing through the ONO layer) and the device almost immediately breaks down. It was reported that the dielectric breakdown was triggered by accumulated holes, but we believe that for our situation, several other causes are possible for the short breakdown time of the ONO layer, especially during the negative-current flow. These include the imperfect interface at the bottom oxide and nitride, the trapped charges in the oxide and the band-bending at the interfaces of polysilicon and oxide, and they are being discussed. (Author abstract) 10 Refs.

24/3,AB/14 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04958675
E.I. No: EIP98034096893
Title: Effect of the floating gate/tunnel SiO//2 interface on **FLASH**

12/06/2002

memory data retention reliability
Author: Kubota, Taishi; Ando, Koichi; Muramatsu, Satoru
Corporate Source: ULSI Device Development Lab
Source: NEC Research & Development v 38 n 4 Oct 1997. p 412-418
Publication Year: 1997
CODEN: NECRAU ISSN: 0547-051X
Language: English
Abstract: The influence of phosphorus at the Floating Gate (FG)/tunnel oxide interface on the **FLASH memory** data retention characteristics is investigated. By measuring the electrical characteristics of memory cells and MOS capacitors, a close relationship was found between the memory cell data retention and Stress Induced Leakage Current (SILC). Lowering the phosphorus density in the FG suppresses SILC and prolongs the data retention. Applying amorphous Si (a-Si) to the FG, in addition, is also found to improve SILC. Thus, the memory cell data retention characteristics is expected to be improved when a-Si is applied to the FG. This a-Si FG advantage is investigated by C-V characteristics, SIMS (Secondary Ion Mass Spectroscopy) and EDX (Energy Dispersive X-Ray Spectroscopy) analysis. In spite of the high impurity activation ratio, the phosphorus concentration at the FG/tunnel oxide interface was confirmed to be lower for the a-Si FG than for the poly-Si FG. Applying a-Si therefore, is confirmed to have the same effect as lowering the phosphorus concentration in the FG but preventing the gate depletion effect. This attractive phenomenon for a-Si may be resulting from the lower phosphorus diffusion along the grain boundary. a-Si therefore will be considered as the promising material for high reliability **FLASH memories**.
(Author abstract) 9 Refs.

24/3,AB/15 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04930438
E.I. No: EIP98024041023
Title: Temperature dependence of TDDB characteristics of thin SiO//2 film for **flash memory**
Author: Katsumata, M.; Teramoto, A.; Kobayashi, K.; Mazumder, M.K.; Sekine, M.; Koyama, H.
Corporate Source: Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1997 6th International Symposium on the Physical & Failure Analysis of Integrated Circuits, IPFA
Conference Location: Singapore, Singapore Conference Date: 19970721-19970725
E.I. Conference No.: 47762
Source: Proceedings of the International Symposium on the Physical & Failure Analysis of Integrated Circuits, IPFA 1997. IEEE, Piscataway, NJ, USA,97TH8289. p 152-155
Publication Year: 1997
CODEN: 002346
Language: English
Abstract: Using a large area capacitor, the temperature dependence of TDDB characteristics for various electric fields was investigated in detail. From the experimental results, it is found that the Qbd value is more dependent on temperature rather than on the electric field. It is also found that the initial breakdown region is divided into two parts, above 175 degree C, the activation energy of the front part of the initial breakdown region is greater than the intrinsic region. It should be possible to use this newly obtained result efficiently to estimate the extrinsic breakdown distribution within a short period during the burn-in test. Therefore, the findings should contribute to the improvement of the

reliability of the actual device. (Author abstract) 5 Refs.

24/3,AB/16 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04744041
E.I. No: EIP97073728456
Title: **FLASH memory** data retention reliability and the floating gate/tunnel SiO//2 interface characteristics
Author: Kubota, Taishi; Ando, Kohichi; Muramatsu, Satore
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 2nd International Symposium on the Control of Semiconductor Interfaces, ISCSI-2
Conference Location: Karuizawa, Jpn Conference Date: 19961028-19961101
E.I. Conference No.: 46599
Source: Applied Surface Science v 117-118 June 2 1997. p 253-258
Publication Year: 1997
CODEN: ASUSEE ISSN: 0169-4332
Language: English
Abstract: The influence of phosphorus at the floating gate (FG)/tunnel oxide interface on the **FLASH memory** data retention characteristics is investigated. By measuring the electrical characteristics of memory cells and MOS capacitors, a close relationship was found between the memory cell data retention and stress induced leakage current (SILC). Lowering the phosphorus density in the FG suppresses SILC and prolong the data retention. Applying amorphous Si (a-Si) to the FG, in addition is also found to improve SILC. Thus the memory cell data retention characteristics are expected to be improved when a-Si is applied to the FG. This a-Si FG advantage is investigated by C-V characteristics, SIMS and EDX analysis. In spite of the high impurity activation ratio, the phosphorous concentration at the FG/tunnel oxide interface was confirmed to be lower for the a-Si FG than for the poly-Si FG. Applying a-Si therefore, is confirmed to have the same effect as lowering the phosphorus concentration in the FG but preventing the gate depletion effect. This attractive phenomenon for a-Si may result from the lower phosphorus diffusion along the grain boundary. a-Si therefore is the most promising material for high reliability **FLASH memories**. (Author abstract) 9 Refs.

24/3,AB/17 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04485028
E.I. No: EIP96083299909
Title: Proceedings of the 1996 Biennial IEEE International Nonvolatile Memory Technology Conference
Author: Anon (Ed.)
Conference Title: Proceedings of the 1996 Biennial IEEE International Nonvolatile Memory Technology Conference
Conference Location: Albuquerque, NM, USA Conference Date: 19960624-19960626
E.I. Conference No.: 45213
Source: Biennial IEEE International Nonvolatile Memory Technology Conference 1996. IEEE, Piscataway, NJ, USA,96TH8200. 142p
Publication Year: 1996
CODEN: 002425
Language: English
Abstract: The proceedings contains 28 papers. Topics discussed include

nonvolatile magnetic memory, mobile computing, ultra-high density memory, optical **memory** devices, **flash memory** architecture, semiconductor devices, **silica** films, mass storage media.

24/3,AB/18 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11147504 Genuine Article#: 610XK Number of References: 25
Title: Three-dimensional self-consistent simulation of the charging time response in silicon nanocrystal **flash memories** (ABSTRACT AVAILABLE)
Author(s): de Sousa JS (REPRINT) ; Thean AV; Leburton JP; Freire VN
Corporate Source: Univ Illinois,Beckman Inst,405 N Mathews Ave/Urbana//IL/61801 (REPRINT); Univ Illinois,Beckman Inst,Urbana//IL/61801; Motorola Inc,Austin//TX/78727; Univ Fed Ceara,Dept Fis,BR-60455760 Fortaleza/Ceara/Brazil/
Journal: JOURNAL OF APPLIED PHYSICS, 2002, V92, N10 (NOV 15), P6182-6187
ISSN: 0021-8979 Publication date: 20021115
Publisher: AMER INST PHYSICS, CIRCULATION & FULFILLMENT DIV, 2 HUNTINGTON QUADRANGLE, STE 1 N O 1, MELVILLE, NY 11747-4501 USA
Language: English Document Type: ARTICLE
Abstract: A numerical model to calculate the tunneling time from the channel of a metal-oxide-semiconductor device into a silicon nanocrystal embedded in **SiO2** is presented. Self-consistent simulations of the Kohn-Sham and Poisson equations are performed to study the role of the size, shape, and barrier thickness of a quantum dot (QD). We found that the charging process is very sensitive to the shape of the QD, resulting in changes of several orders of magnitude in the electron transfer and retention times. (C) 2002 American Institute of Physics.

24/3,AB/19 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

11114009 Genuine Article#: 609ED Number of References: 20
Title: Evaluation methodology of thin dielectrics for non-volatile memory application (ABSTRACT AVAILABLE)
Author(s): Ghidini G (REPRINT) ; Brazzelli D
Corporate Source: STMicroelect,Cent R&D,Via C Olivetti 2/I-20041 Agrate Brianza//Italy/ (REPRINT); STMicroelect,Cent R&D,I-20041 Agrate Brianza//Italy/
Journal: MICROELECTRONICS RELIABILITY, 2002, V42, N9-11 (SEP-NOV), P 1473-1480
ISSN: 0026-2714 Publication date: 20020900
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: The quality of active dielectrics and in particular of tunnel oxide has a strong impact on **Flash memory** yield and reliability. For this reason, major efforts are required to improve active oxide characterisation methodology.

A monitor of extrinsic defects and local dielectric thinning is crucial to improve device yield and tighten threshold distributions. Besides, deeper characterizations are necessary for correlating device and simple structures intrinsic degradation during cycling. This is mostly important when introducing new fabrication process steps.

Moreover, high temperature data retention is directly correlated to the quality of all dielectrics surrounding the floating gate. The interpoly dielectric is the most critical from this point of view: a methodology to monitor the dielectric thickness and composition will be presented.

Finally, the reduction of tunnel oxide thickness below 10 nm causes the onset of Stress Induced Leakage Current (SILC). In most recent technologies this causes problems of single bit charge loss at room temperature after cycling. A characterization of the phenomenon on simple structures is here reported, allowing a better understanding of the failure mechanisms. Key parameters are pointed out, although without reproducing the observed anomalous leakage currents found only in a few cells of real devices.

24/3,AB/20 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10597565 Genuine Article#: 545UE Number of References: 31
Title: Damage generation and location in n- and p-MOSFETs biased in the substrate-enhanced gate current regime (ABSTRACT AVAILABLE)
Author(s): Driussi F (REPRINT) ; Esseni D; Selmi L; Piazza F
Corporate Source: ST Microelect,Agrate Brianza//Italy/ (REPRINT); ST Microelect,Agrate Brianza//Italy/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 2002, V49, N5 (MAY), P 787-794
ISSN: 0018-9383 Publication date: 20020500
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: This paper analyzes MOSFET degradation in the regime of hot carrier injection enhanced by substrate bias Substrate-Enhanced Gate Current (SEGC). The results are compared with the damage generated during conventional Channel Hot Carrier (CHC) stress experiments.

The investigation was carried out on state of the art n(+)-poly n-MOSFETs and p(+)-poly p-MOSFETs, and it includes both a detailed characterization of standard electrical parameters (i.e., threshold voltage, drain current and linear transconductance) and a spatial profiling of stress-induced interface states.

Our results reveal that the application of a substrate bias enhances degradation on both n-MOS and p-MOS devices and spreads toward the center of the channel the spatial profile of the damage. For a given gate current and oxide field in the injection region, the total amount of the generated damage is quite similar in both cases, but in the SEGC regime, the spatial distribution of generated traps is more distributed along the channel.

24/3,AB/21 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10365352 Genuine Article#: 517MQ Number of References: 4
Title: JVD silicon nitride as tunnel dielectric in p-channel **flash memory** (ABSTRACT AVAILABLE)

Author(s): She M (REPRINT) ; King TJ; Hu CM; Zhu WJ; Luo ZJ; Han JP; Ma TP
Corporate Source: Univ Calif Berkeley,Dept Elect Engn & Comp Sci,Berkeley//CA/94720 (REPRINT); Univ Calif Berkeley,Dept Elect Engn & Comp Sci,Berkeley//CA/94720; Yale Univ,Ctr Microelect Mat & Struct,New Haven//CT/06520; Yale Univ,Dept Elect Engn,New Haven//CT/06520
Journal: IEEE ELECTRON DEVICE LETTERS, 2002, V23, N2 (FEB), P91-93
ISSN: 0741-3106 Publication date: 20020200
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: High-quality jet vapor deposition nitride is investigated as a tunnel dielectric for **flash memory** device application. Compared to control devices with **SiO2** tunnel dielectric, faster programming speed as well as better retention time are achieved with low programming voltage. The p-channel devices can be programmed by hot electrons and erased by hot holes, or vice versa. Multilevel programming capability is shown.

24/3,AB/22 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10198947 Genuine Article#: BT24Z Number of References: 12
Title: Monitoring of defects in thermal oxides during electrical stress (ABSTRACT AVAILABLE)
Author(s): Caputo D (REPRINT) ; Irrera F; Palma F
Corporate Source: Dept Elect Engn Rome La Sapienza,Via Eudossiana 18/IT-00185 Rome//Italy/ (REPRINT); Dept Elect Engn Rome La Sapienza,IT-00185 Rome//Italy/
, 2002, V82-84, P237-242
ISSN: 1012-0394 Publication date: 20020000
Publisher: TRANS TECH PUBLICATIONS LTD, BRANDRAIN 6, CH-8707 ZURICH-UETIKON, SWITZERLANDGETTERING AND DEFECT ENGINEERING IN SEMICONDUCTOR TECHNOLOGY
Series: SOLID STATE PHENOMENA
Language: English Document Type: ARTICLE
Abstract: A detailed monitoring of stressed thermal oxide designed for **Flash memories** application is reported The samples were stressed through a constant current injection and characterized by current-voltage and capacitance-voltage measurements at different steps of degradation. Low-frequency capacitance measurements under substrate accumulation have been also performed and interpreted by a model which takes into account the contribution to capacitance given by trapped charge moving between defects under a small signal perturbation. Results obtained in deposited oxide are also reported.

24/3,AB/23 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10188220 Genuine Article#: 495TQ Number of References: 6
Title: Electrical degradation and recovery of dielectrics in n(++)-poly-Si/SiOx/**SiO2**/p-sub structures designed for application in low-voltage non-volatile memories (ABSTRACT AVAILABLE)
Author(s): Irrera F (REPRINT)
Corporate Source: Univ Roma La Sapienza,Dept Elect,Via Eudossiana 18/I-00184 Rome//Italy/ (REPRINT); Univ Roma La Sapienza,Dept Elect,I-00184 Rome//Italy/
Journal: MICROELECTRONICS RELIABILITY, 2001, V41, N11 (NOV), P1809-1813

ISSN: 0026-2714 Publication date: 20011100
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: In this paper we Study the degradation and recovery of dielectrics in n(++)-poly-Si/SiOx/**SiO2**/p-sub capacitors designed for application in low-voltage **flash** EEPROM **memories**. Constant current stress experiment have been performed and the gate voltage in the Fowler-Nordheim (FN) regime and the flat-band voltage monitored. Experiment demonstrated that SiOx has a greater tendency to trap electrons than pure **SiO2** and exhibits a larger voltage shift in the FN regime after electrical stress. On the other hand, permanent recovery of the leakage current can be obtained by injection of current at very low flux. This effect has been tentatively explained with the annealing of native metastable defects occurring in concurrence with the stress induced creation of new traps, (C) 2001 Elsevier Science Ltd. All rights reserved.

24/3,AB/24 (Item 7 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09261843 Genuine Article#: 384HB Number of References: 18
Title: Fabrication technology of a Si nanowire memory transistor using an inorganic electron beam resist process (ABSTRACT AVAILABLE)
Author(s): Tsutsumi T (REPRINT) ; Ishii K; Hiroshima H; Hazra S; Yamanaka M ; Sakata I; Taguchi H; Suzuki E; Tomizawa K
Corporate Source: Electrotech Lab,Electron Devices Div,1-1-4 Umezono/Tsukuba/Ibaraki 3058568/Japan/ (REPRINT); Electrotech Lab,Electron Devices Div,Tsukuba/Ibaraki 3058568/Japan/; Meiji Univ,Tama Ku,Kawasaki/Kanagawa 2148571/Japan/
Journal: JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B, 2000, V18, N6 (NOV-DEC) , P2640-2645
ISSN: 1071-1023 Publication date: 20001100
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501 USA
Language: English Document Type: ARTICLE
Abstract: We report on a novel fabrication technology of a Si nanowire memory transistor using an inorganic **SiO2** electron beam (EB) resist process. The inorganic EB resist process technique was put to practical use in Si nanodevice fabrication for the first time. We have successfully demonstrated the 15-nm-wide and 20-nm-thick Si nanowire memory transistor with a Si nanodot less than 10 nm in diameter. In the fabricated Si nanowire nanodot memory transistor, we have observed a large electron memory effect, i.e., a threshold voltage shift DeltaV(th) of 2.2 V at room temperature. It is experimentally shown that the inorganic EB resist process is promising for fabricating various Si nanodevices. (C) 2000 American Vacuum Society. [S0734-211X(00)03306-0].

24/3,AB/25 (Item 8 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08671490 Genuine Article#: 314WZ Number of References: 11
Title: On the origin of the dispersion of erased threshold voltages in **flash** EEPROM **memory** cells (ABSTRACT AVAILABLE)
Author(s): Esseni D (REPRINT) ; Ricco B
Corporate Source: UNIV BOLOGNA,DEIS/I-40136 BOLOGNA//ITALY/ (REPRINT)

12/06/2002

Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 2000, V47, N5 (MAY), P 1120-1123
ISSN: 0018-9383 Publication date: 20000500
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: This work investigates the origin of the dispersion of tunnel-erased threshold voltages (V-T) in **flash** EEPROM **memory** cells. A clear correlation between cell-to-cell variations of tunnel current I-T. and dispersion of erased V-T is demonstrated by looking at the I-T characteristics and the erasing characteristics corresponding to channel and source injection as well as at the dependence of I-T and V-T dispersion on device area and tunnel polarity. Experimental evidence is provided that nonuniform injection at polySi/**SiO2** interface is a major cause of erased V-T dispersion.

24/3,AB/26 (Item 9 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08609722 Genuine Article#: 307VN Number of References: 16
Title: Development of a low-cost tide gauge (ABSTRACT AVAILABLE)
Author(s): Giardina MF (REPRINT) ; Earle MD; Cranford JC; Osiecki DA
Corporate Source: NEPTUNE SCI INC,40201 HIGHWAY 190 E/SLIDELL//LA/70461 (REPRINT)
Journal: JOURNAL OF ATMOSPHERIC AND OCEANIC TECHNOLOGY, 2000, V17, N4 (APR), P575-583
ISSN: 0739-0572 Publication date: 20000400
Publisher: AMER METEOROLOGICAL SOC, 45 BEACON ST, BOSTON, MA 02108-3693
Language: English Document Type: ARTICLE
Abstract: A low-cost tide gauge was developed and field tested to demonstrate a technology that would enable more cost-effective and greater sampling of spatially variable water levels and ocean surface waves. The gauge was designed to be adaptable to expendable and, possibly, air-deployed use for applications such as support of naval operations. The gauge incorporates a single printed circuit board that includes a very low power 3.3-Vdc microprocessor and 1 Mbyte of nonvolatile **flash memory**. A low-cost solid-state pressure sensor provides pressure data that are corrected automatically as a function of measured pressure and temperature and are processed within the gauge to provide low-frequency water levels and nondirectional surface wave information. Gauge-operating lifetimes range from more than four months to more than two years, depending on the data collection mode (tide or tide-wave) and the data collection interval (half-hourly or hourly). Gauge measurements are compared to measurements from a Sea-Bird Electronics, Inc., wave and tide gauge that uses a high quality **quartz** sensor.

24/3,AB/27 (Item 10 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08484730 Genuine Article#: 287WK Number of References: 15
Title: High spatial density nanocrystal formation using thin layer of amorphous Si0.7Ge0.3 deposited on **SiO2** (ABSTRACT AVAILABLE)
Author(s): Yoon TS (REPRINT) ; Kwon JY; Lee DH; Kim KB; Min SH; Chae DH; Kim DH; Lee JD; Park BG; Lee HJ
Corporate Source: SEOUL NATL UNIV,SCH MAT SCI & ENGN/SEOUL 151742//SOUTH

KOREA/ (REPRINT); KANGNUNG NATL UNIV,DEPT MET ENGN/KANGNUNG 210702//SOUTH KOREA/; SEOUL NATL UNIV,SCH ELECT ENGN/SEOUL 151742//SOUTH KOREA/; KOREA RES INST STAND & SCI,NEW MAT EVALUAT CTR/TAEJON 305600//SOUTH KOREA/
Journal: JOURNAL OF APPLIED PHYSICS, 2000, V87, N5 (MAR 1), P2449-2453
ISSN: 0021-8979 Publication date: 20000301
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501
Language: English Document Type: ARTICLE
Abstract: The process to make nanocrystals with an average size < 5 nm and a spatial density > 10(12)/cm(2) was proposed using agglomeration and partial oxidation of thin amorphous Si0.7Ge0.3 layer deposited in between the **SiO2** layers by low pressure chemical vapor deposition. The reason to use an amorphous layer is to make it possible to deposit a thin continuous layer with a thickness of less than 5 nm. Si0.7Ge0.3 alloy layer was used to control the spatial density of the nanocrystals by using selective oxidation of Si in Si0.7Ge0.3 alloy layer. The single electron memory, similar to a **flash** type **memory** device was fabricated using these Si0.7Ge0.3 nanocrystals. The Coulomb blockade effect could be clearly observed at room temperature with a threshold voltage shift of about 2.4 V, which demonstrated the formation of nanocrystals with a high spatial density. (C) 2000 American Institute of Physics. [S0021-8979(00)06405-7].

24/3,AB/28 (Item 11 from file: 34)

08365884 Genuine Article#: 277CR Number of References: 30
Title: Electrically and radiation induced leakage currents in thin oxides (ABSTRACT AVAILABLE)
Author(s): Scarpa A; Riess P; Ghibaudo G (REPRINT) ; Paccagnella A; Pananakakis G; Ceschia M; Ghidini G
Corporate Source: CNRS,UMR, INPG, ENSERG, LAB PHYS COMPOSANTS SEMICOND, BP 257, 23 RUE MARTYRS/F-38016 GRENOBLE//FRANCE/ (REPRINT); CNRS,UMR, INPG, ENSERG, LAB PHYS COMPOSANTS SEMICOND/F-38016 GRENOBLE//FRANCE/; DEIV PADUA,/I-35131 PADUA//ITALY/; ST MICROELECT,CENT R&D/I-20041 AGRATE BRIANZA//ITALY/
Journal: MICROELECTRONICS RELIABILITY, 2000, V40, N1 (JAN), P57-67
ISSN: 0026-2714 Publication date: 20000100
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: Stress Induced Leakage Current (SILC) has been recognized as a topic of concern in **flash memory** reliability. It is a veritable failure mechanism, occurring long before oxide breakdown and, hence, limiting oxide lifetime. The physical origin and mechanisms of SILC have not yet been clearly understood and several open points to discussion remain, In this work the electrical characteristics of SILC have been studied and an empirical reliability model for ultra-thin gate oxide has been proposed. Moreover, ionizing radiation effects in leakage current generation have been analyzed and compared to electrical SILC, (C) 2000 Elsevier Science Ltd. All rights reserved.

24/3,AB/29 (Item 12 from file: 34)

06736097 Genuine Article#: ZN627 Number of References: 57

12/06/2002

Title: Gate oxide defects in MOSLSIs and octahedral void defects in Czochralski silicon (ABSTRACT AVAILABLE)
Author(s): Itsumi M (REPRINT) ; Ueki T; Watanabe M; Yabumoto N
Corporate Source: NIPPON TELEGRAPH & TEL PUBL CORP,SYST ELECT LABS, 3-1 MORINOSATO WAKAMIYA/ATSUGI/KANAGAWA 24301/JAPAN/ (REPRINT); NIPPON TELEGRAPH & TEL PUBL CORP,ELECT/ATSUGI/KANAGAWA 24301/JAPAN/; NIPPON TELEGRAPH & TEL PUBL CORP,ADV TECHNOL/ATSUGI/KANAGAWA 24301/JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1998, V37, N3B (MAR), P1228-1235
ISSN: 0021-4922 Publication date: 19980300
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: The origin of insulator defects in gate oxides and poly-oxides was thoroughly investigated. We clarified that octahedral void defects originating in a Czochralski silicon substrate are responsible for gate-oxide defects and that polyhedral void defects produced during annealing or oxidation are responsible for defects in insulators on poly-silicon. These are expected to be the principal defects affecting the yield and reliability of next-generation metal-oxide-silicon large-scale integrated-circuits or **flash memories**. In addition, defects in the buried oxides of a silicon-on-insulator substrate were also examined. Octahedral defects or polyhedral defects were observed just under the buried-oxide defects. Octahedral defects and polyhedral defects may be common in standard metal-oxide-silicon large-scale integrated-circuits, **flash memories**, and silicon-on-insulator substrates.

24/3,AB/30 (Item 13 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06560816 Genuine Article#: ZB120 Number of References: 26
Title: Origin of thin-oxide defects affecting yield and reliability of floating-gate devices and **flash memories** (ABSTRACT AVAILABLE)
Author(s): Itsumi M (REPRINT) ; Akiya H; Tomita M; Ueki T; Yamawaki M
Corporate Source: NIPPON TELEGRAPH & TEL PUBL CORP,SYST ELECT LABS/KANAGAWA 24301//JAPAN/ (REPRINT); NIPPON TELEGRAPH & TEL PUBL CORP,SCI & CORE TECHNOL LAB GRP/KANAGAWA 24301//JAPAN/; NIPPON TELEGRAPH & TEL PUBL CORP,SCI & CORE TECHNOL LAB GRP/TOKYO 180//JAPAN/; NIPPON TELEGRAPH & TEL PUBL CORP,ELECT CORP/KANAGAWA 24301//JAPAN/; NIPPON TELEGRAPH & TEL PUBL CORP,ADV TECHNOL CORP/TOKYO 180//JAPAN/
Journal: SOLID-STATE ELECTRONICS, 1998, V42, N1 (JAN), P107-113
ISSN: 0038-1101 Publication date: 19980100
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD, ENGLAND OX5 1GB
Language: English Document Type: ARTICLE
Abstract: Gate-oxide and inter-gate-oxide defects in floating-gate transistors and hash memories, the number of which has been minimized but is still not zero, have been examined extensively. Gate-oxide defects are due to 0.1 mu m size octahedral void pits at the Si surface. They are originally grown-in defects in the Si crystal and appear as surface pits when they are truncated at the surface when wafers are sliced and polished. On the other hand, inter-gate oxide defects are due to polygonal-shaped voids at the poly-silicon grain boundary. These defects are produced as a negative crystal in the crystallization process of amorphous Si during annealing. Methods for eliminating the above defects are suggested. (C) 1998 Elsevier Science Ltd. All rights reserved.

24/3,AB/31 (Item 14 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06082663 Genuine Article#: XT996 Number of References: 83
Title: **Flash memory** cells - An overview (ABSTRACT AVAILABLE)
Author(s): Pavan P (REPRINT) ; Bez R; Olivo P; Zanoni E
Corporate Source: UNIV MODENA,DIPARTIMENTO SCI INGN/I-41100 MODENA//ITALY/ (REPRINT); SGS THOMSON MICROELECT,CENT RES & DEV/I-20041 AGRATE BRIANZA/MI/ITALY/; UNIV FERRARA,DIPARTIMENTO ENGN/I-44100 FERRARA//ITALY/; UNIV PADUA,DIPARTIMENTO ELETTRON & INFORMAT/I-35131 PADUA//ITALY/
Journal: PROCEEDINGS OF THE IEEE, 1997, V85, N8 (AUG), P1248-1271
ISSN: 0018-9219 Publication date: 19970800
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: The aim of this paper is to give a thorough overview of **Flash memory** cells. Basic operations and charge-injection mechanisms that are most commonly used in actual **Flash memory** cells are reviewed to provide an understanding of the underlying physics and principles in order to appreciate the large number of device structures, processing technologies, and circuit designs presented in the literature. New cell structures and architectural solutions have been surveyed to highlight the evolution of the **Flash memory** technology, oriented to both reducing cell size and upgrading product functions. The subject is of extreme interest: new concepts involving new materials, structures, principles, or applications are being continuously introduced. The worldwide semiconductor memory market seems ready to accept many new applications in fields that are not specific to traditional nonvolatile memories.

24/3,AB/32 (Item 15 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05987295 Genuine Article#: XM441 Number of References: 9
Title: Improvement of the tunnel oxide quality by a low thermal budget dual oxidation for **flash memories** (ABSTRACT AVAILABLE)
Author(s): Kim J (REPRINT) ; Ahn ST
Corporate Source: SAMSUNG ELECT CO LTD,MEMORY DIV/KYUNGKI 449900//SOUTH KOREA/ (REPRINT)
Journal: IEEE ELECTRON DEVICE LETTERS, 1997, V18, N8 (AUG), P385-387
ISSN: 0741-3106 Publication date: 19970800
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: The high-quality ultrathin tunnel oxide using a low thermal budget dual oxidation has been developed. Due mainly to the reduction of imperfect chemical bonds and interface roughness, the tunnel and gate oxide quality in the fabrication of **flash memory** such as stress-induced leakage current (SILC), effective electron mobility, and cycling endurance characteristics, were improved compared to the pure dry oxides.

24/3,AB/33 (Item 16 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

12/06/2002

05938874 Genuine Article#: XJ055 Number of References: 8
Title: Feasibility of steam tunnel oxide for advanced non volatile memories (ABSTRACT AVAILABLE)
Author(s): Ghidini G (REPRINT) ; Tosi M; Clementi C
Corporate Source: SGS THOMSON MICROELECT,CENT R&D, VIA C OILVETTI 2/I-20041 AGRATE BRIANZA//ITALY/ (REPRINT)
Journal: SOLID-STATE ELECTRONICS, 1997, V41, N7 (JUL), P975-979
ISSN: 0038-1101 Publication date: 19970700
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD, ENGLAND OX5 1GB
Language: English Document Type: ARTICLE
Abstract: In order to reduce dopant diffusion to obtain device scaling, a decrease of any thermal treatment is required. Therefore, to substitute dry thermal oxides for tunnel application in **Flash Memories**, the possibility of using steam oxides grown at low temperatures was studied, considering, in addition, scaling of these oxides for future generations. Results concerning oxide reliability and charge trapping for elementary structures are presented and correlated with device performance. (C) 1997 Elsevier Science Ltd.

24/3,AB/34 (Item 17 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05623751 Genuine Article#: WL647 Number of References: 9
Title: Electrical characterization of highly reliable 8 nm oxide (ABSTRACT AVAILABLE)
Author(s): Ghidini G (REPRINT) ; Alessandri M; Clementi C; Drera D; Pellizzer F
Corporate Source: SGS THOMSON MICROELECT,/I-20041 AGRATE BRIANZA//ITALY/ (REPRINT)
Journal: JOURNAL OF THE ELECTROCHEMICAL SOCIETY, 1997, V144, N2 (FEB), P 758-764
ISSN: 0013-4651 Publication date: 19970200
Publisher: ELECTROCHEMICAL SOC INC, 10 SOUTH MAIN STREET, PENNINGTON, NJ 08534
Language: English Document Type: ARTICLE
Abstract: Device scaling down requires the decreasing of any thermal treatment in order to reduce dopant diffusion. The possibility of using steam oxides grown at low temperatures to substitute dry thermal oxides for tunnel application in **flash memory** is investigated here comparing different technologies: standard dry/steam and N2O nitrided dry/steam oxides. A direct comparison in terms of oxide defect level and breakdown characteristics is presented, also considering the charge trapping behavior of area and periphery capacitors. A correlation between residual charge trapping and intrinsic reliability of these oxides is also presented, showing that the overall best performances are obtained by the nitrided oxides. The nitridation of steam oxide at high temperature results in good charge trapping characteristics, comparable with those of a nitrided dry oxide; at the same time charge-to-breakdown improves, while the defect level decreases. In the investigated thickness range even the nitridation of a steam oxide at low temperature resulted in a suitable dielectric for tunnel application in **flash memories**.

24/3,AB/35 (Item 18 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

12/06/2002

04986595 Genuine Article#: UX140 Number of References: 20
Title: EXCELLENT EMISSION CHARACTERISTICS OF TUNNELING OXIDES FORMED USING ULTRATHIN SILICON FILMS FOR **FLASH MEMORY** DEVICES (Abstract Available)
Author(s): WANG PW; KU TK; SU HP; HONG G; CHENG HC
Corporate Source: NATL CHIAO TUNG UNIV,DEPT ELECTR ENGN/HSINCHU//TAIWAN/; NATL CHIAO TUNG UNIV,SEMICOND RES CTR,INST ELECTR/HSINCHU//TAIWAN/; UNITED MICROELECT CORP/HSINCHU//TAIWAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1996, V35, N6A (JUN), P3369-3373
ISSN: 0021-4922
Language: ENGLISH Document Type: ARTICLE
Abstract: A novel technique using oxidized ultrathin rugged polysilicon films on silicon substrates has been appied to significantly improve the tunneling efficiency of thin oxides. As compared with oxidized amorphous silicon films, these rugged polysilicon films can achieve a higher emission current. High-resolution transmission electron microscopy (HRTEM) was used to observe the atomic-scale microtips at the **SiO2**/Si and polysilicon/**SiO2** interfaces. According to the extracted geometry parameters of the microtips, a two-dimensional numerical simulator based on the finite difference method using the curved emitting surface of microtips can well explain the remarkable current asymmetry of the dielectrics. This suggests that the oxidized rugged polysilicon films can form higher microtips and smaller tip angles, resulting in better emission characteristics that will enable potential applications to future 5-V-only nonvolatile memories.

24/3,AB/36 (Item 19 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04101741 Genuine Article#: RE530 Number of References: 13
Title: AN ANALYTICAL MODEL FOR THE OPTIMIZATION OF SOURCE-SIDE INJECTION FLASH EEPROM DEVICES (Abstract Available)
Author(s): VANHOUDT JF; GROESENEKEN G; MAES HE
Corporate Source: INTERUNIV MICROELECTR CTR,KAPELDREEF 75/B-3001 LOUVAIN//BELGIUM/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1995, V42, N7 (JUL), P 1314-1320
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Abstract: This paper presents an analytical model for the description of the programming operation in split-gate source-side injection **Flash memory** devices, From a dual-gate MOS model and from device simulations, it is found that the lateral field is almost independent of the floating-gate voltage which focuses the description of the gate current during programming on the physics of the Si-**SiO2** barrier lowering effect. The traditional Lucky Electron Model [1] is used to accurately describe the gate current and, therefrom, the programming characteristic is calculated analytically with a minor approximation, The validity and the usefulness of the model for device design purposes is demonstrated by comparing the results to experimental data obtained from Flash EEPROM cells fabricated in a 1.2 mu m and a 0.7 mu m technology, respectively.

24/3,AB/37 (Item 20 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

12/06/2002

03888815 Genuine Article#: QN571 Number of References: 48
Title: THIN OXIDE ON SI (Abstract Available)
Author(s): OHIJ Y; USHIYAMA M
Corporate Source: HITACHI LTD,CENT RES LAB,1-280 HIGASHI KOIGAKUBO/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: JOURNAL OF THE KOREAN PHYSICAL SOCIETY, 1995, V28, S (FEB), PS1-S7
ISSN: 0374-4884
Language: ENGLISH Document Type: ARTICLE
Abstract: Charge trapping phenomena and TDDB characteristics in thin gate **SiO2** film of advanced MOS devices have been investigated. The electron trapping is strongly related to the SiOH or SIH bond in the **SiO2** films, while the hole trapping is caused by formation of oxygen vacancy in the **SiO2**. There is a seesaw relationship between the hole trap density and the electron trap density, and accordingly, we can not expect to reduce the electron trap and the hole trap simultaneously. We found that the oxynitridation of **SiO2** film decreased both the electron traps and the hole traps in the **SiO2**. This oxynitried **SiO2** gate dielectric improved in the programming time degradation during program/erase cyclic operations of the **flash-memory**.

24/3,AB/38 (Item 21 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03673751 Genuine Article#: PW329 Number of References: 2
Title: CHARACTERIZATION OF FLASH STRUCTURES ERASED WITH ULTRASHORT PULSES (Abstract Available)
Author(s): LANZONI M; RIVA C; OLIVO P
Corporate Source: UNIV BOLOGNA,DEIS,VLE RISORGIMENTO 2/I-40136 BOLOGNA//ITALY/; SGS THOMSON MICROELECTR/I-20041 AGRATE BRIANZA//ITALY/
Journal: MICROELECTRONICS JOURNAL, 1994, V25, N7 (OCT), P491-494
ISSN: 0026-2692
Language: ENGLISH Document Type: ARTICLE
Abstract: **Flash memories** are normally erased by means of high-field electron tunnelling from the floating gate into the source. As a consequence the time needed is generally two orders of magnitude larger (approximate to 1 ms vs. approximate to 10 mu s) than that used for writing, and is obtained by means of much higher currents due to channel hot electrons. It is important therefore to determine whether it is possible to reduce the erase time, in order to make it comparable with that used for writing. With regard to such a problem, this work describes the results of a comprehensive and detailed characterization of flash structures aimed at evaluating how ultra-short, high voltage erasing pulses affect the reliability of the device.

24/3,AB/39 (Item 22 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02650692 Genuine Article#: LU166 Number of References: 14
Title: SUCCESSIVE CHARGING DISCHARGING OF GATE OXIDES IN SOI MOSFETS BY SEQUENTIAL HOT-ELECTRON STRESSING OF FRONT BACK CHANNEL (Abstract Available)
Author(s): ZALESKI A; IOANNOU DE; CAMPISI GJ; HUGHES HL
Corporate Source: GEORGE MASON UNIV,DEPT ELECT & COMP ENGN/FAIRFAX//VA/22030; USN,RES LAB/WASHINGTON//DC/20375

12/06/2002

Journal: IEEE ELECTRON DEVICE LETTERS, 1993, V14, N9 (SEP), P435-437
ISSN: 0741-3106
Language: ENGLISH Document Type: ARTICLE
Abstract: Hot-hole injection into the opposite channel of SOI MOSFET's under hot-electron stress is reported. Sequential front/back-channel hot-electron stressing results in successive hot-electron/hole injection, causing the threshold voltage to increase and decrease accordingly. This ability to inject hot holes into the opposite gate oxide can be used as an additional tool for studying the degradation mechanisms. Furthermore, it may be explored for possible use in designing SOI **flash memory** cells with back-channel-based erasing schemes.

24/3,AB/40 (Item 23 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01780433 Genuine Article#: JA386 Number of References: 13
Title: DESIGN, SELECTION AND IMPLEMENTATION OF **FLASH** ERASE EEPROM **MEMORY** CELLS (Abstract Available)
Author(s): AMIN AAM
Corporate Source: KING FAHD UNIV PETR & MINERALS,DEPT COMP ENGN/DHAHRAN 31261//SAUDI ARABIA/
Journal: IEE PROCEEDINGS-G CIRCUITS DEVICES AND SYSTEMS, 1992, V139, N3 (JUN), P370-376
Language: ENGLISH Document Type: ARTICLE
Abstract: The paper reports an investigation into the design and process constraints of **FLASH** EEPROM **memory** cells. It describes several possible structures which were developed by the MOS memory R&D group of National Semiconductor Corporation at West Jordan, Utah. These structures were implemented and tested on a specially designed test chip. In addition to the typical structures of poly 1 floating gate and poly 2 control gate, new novel structures of poly 2 floating gate and poly 1 control gate were implemented. A total of 5 major structures are described. The paper discusses the principle of operation, advantages and disadvantages of each of these structures. It also includes characteristic results and discussion of the performance of these candidate cells.

24/3,AB/41 (Item 1 from file: 434)
DIALOG(R)File 434:SciSearch(R) Cited Ref Sci

09333837 Genuine Article#: T3836 Number of References: 9
Title: DEGRADATIONS DUE TO HOLE TRAPPING IN **FLASH MEMORY** CELLS
Author(s): HADDAD S; CHANG C; SWAMINATHAN B; LIEN J
Corporate Source: ADV MICRO DEVICES INC/SUNNYVALE//CA/94088
Journal: IEEE ELECTRON DEVICE LETTERS, 1989, V10, N3, P117-119
Language: ENGLISH Document Type: ARTICLE

24/3,AB/42 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04168477 JICST ACCESSION NUMBER: 99A0591287 FILE SEGMENT: JICST-E
TCAD for Semiconductor Indutries. 2-Dimensional Simulation of FN Current Suppression Including Phonon Assisted Tunneling Model in **Silicon Dioxide**.

12/06/2002

EIKYU K (1); SAKAKIBARA K (1); ISHIKAWA K (1); NISHIMURA T (1)
(1) Mitsubishi Electric Corp., Itami-shi, Jpn
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1999, VOL.E82-C,NO.6, PAGE.889-893, FIG.9, REF.10
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A gate oxide excess current model is described based on the phonon-assisted tunneling ptocess of electrons into neutral traps. The influence on local electric field of charge of electrons trapped by neutral traps in gate oxide is simulated using a two-dimensional device simulator into which the new model is incorporated. FN current is suppressed with an increase in the, neutral trap density to over 1019cm-3. The calculated results reflect the endurance characteristics of **flash memories** in which erase/write operation speed depends on FN current. (author abst.)

24/3,AB/43 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02901582 JICST ACCESSION NUMBER: 97A0503703 FILE SEGMENT: PreJICST-E
Application of NH3 Annealed CVD **SiO2** Single Films to Interpoly Dielectrics of **Flash Memories**.
KATAYAMA ATSUKO (1); KOBAYASHI TAKASHI (1); KUME HITOSHI (1); KIMURA KATSUTAKA (1)
(1) Hitachi, Ltd., Cent. Res. Lab.
Oyo Butsurigaku Kankei Rengo Koenkai Koen Yokoshu, 1997, VOL.44th,NO.2, PAGE.723
JOURNAL NUMBER: Y0054AAR
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
MEDIA TYPE: Printed Publication

24/3,AB/44 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02139347 JICST ACCESSION NUMBER: 95A0555404 FILE SEGMENT: PreJICST-E
Influence of **SiO2**/Si interface roughness on Vt distribution after erase in **flash memory**.
NAKAGAWA KEN'ICHIRO (1); TSUKIJI MASARU (1); KAWADA MASATO (1); OKAZAWA TAKESHI (1)
(1) NEC Corp.
Oyo Butsurigaku Kankei Rengo Koenkai Koen Yokoshu, 1995, VOL.42nd,NO.Pt 2, PAGE.829
JOURNAL NUMBER: Y0054AAR
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
MEDIA TYPE: Printed Publication

24/3,AB/45 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

12/06/2002

01988386 JICST ACCESSION NUMBER: 94A0276675 FILE SEGMENT: JICST-E
Numerical Analysis of Tunneling Current due to Electric Field Concentration at Gate Edge of Polysilicon/**SiO2**/Silicon Structures.
MUTO H (1); KITABAYASHI H (1); NAKANISHI K (1); WAKE S (1); NAKAJIMA M (1)
(1) Mitsubishi Electric Corp., Amagasaki
Jpn J Appl Phys Part 1, 1994, VOL.33,NO.1B, PAGE.623-629, FIG.11, REF.13
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 681.327 621.382 MIS
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Tunneling current enhancement due to electric field concentration at a gate edge is investigated by numerical calculation. The detailed current distribution and change of current-voltage (I-V) characteristics are calculated for several gate geometries differing in curvature radius. It is shown that the current density of an MOS structure with an oxide thickness of 12nm varies by 3 orders of magnitude when the curvature radius at the gate edge changes from 30nm to 2nm. A very narrow region of 8nm at the curvature area is responsible for 80% of the total current between the gate and n+ region. The calculated change in I-V characteristics is consistent with the experimentally measured I-V curve of a polysilicon gate/**SiO2** /n+-silicon structure. (author abst.)

24/3,AB/46 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15760979 PASCAL No.: 02-0473814
ETUDE DE LA CREATION DE PROTONS MOBILES DANS L'OXYDE DE SILICIUM ET APPLICATION A UN SYSTEME DE MEMOIRE NON VOLATILE
(STUDY OF THE PROTON CREATION IN **SILICON DIOXIDE** AND APPLICATION TO A NON-VOLATILE MEMORY DEVICE)
GIRAULT Valerie; PLOSSU Carole, dir
Institut national des sciences appliquees de Lyon, Villeurbanne, France
Univ.: Institut national des sciences appliquees de Lyon. Villeurbanne.
FRA Degree: Th. doct.
2001-01; 2001 232 p.
Language: French Summary Language: French; English
Le developpement et l'optimisation des memoires non volatiles ont conduit a l'emergence des memoires EEPROM et FLASH EEPROM aujourd'hui tres fiables, qui occupent desormais la majeure partie de la production mondiale. Dans le but de proposer un dispositif aussi fiable et consommant encore moins d'energie, l'idee d'un systeme de memoire non volatile a emerge en 1996 ayant pour base la migration de protons mobiles dans l'oxyde de grille d'un transistor MOS. Ces protons sont obtenus par recuit des structures sous hydrogene. C'est donc dans cette perspective que ce travail de these a ete engage. Tout d'abord une etude experimentale exhaustive concernant les conditions de creation de protons mobiles dans l'oxyde de silicium est rapportee. Elle a ete realisee sur des dispositifs elementaires fabriques sur des substrats Silicon On Insulator (SOI), les premiers a avoir permis cet effet. Les premiers dispositifs memoires ayant demontre des caracteristiques prometteuses, l'etape suivante dans cette etude a concerne le remplacement de la structure SOI par une structure similaire realisee avec des procedes et des materiaux plus standards et en particulier avec de l'oxyde de silicium thermique. Cette etape franchie sur des dispositifs capacitifs, nous avons engage la fabrication d'un transistor memoire. L'oxyde thermique a ete utilise et des procedes de realisation ont ete tentes. Si les transistors ont permis, pour une part, de creer les protons

mobiles dans l'oxyde de grille, la caracterisation electrique des dispositifs a mis en evidence des disfonctionnements majeurs qui empechent la fabrication reelle de ce type de memoire non volatile. En revanche, l'etude a permis de mieux comprendre les reactions chimiques entre l'oxyde de silicium et l'hydrogene, ces deux composants restant tres presents dans les procedes technologiques de la microelectronique d'aujourd'hui.

24/3,AB/47 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

13405331 PASCAL No.: 98-0097793
The effect of the Floating Gate/tunnel SiO SUB 2 interface on **FLASH memory** data retention reliability
KUBOTA T; ANDO K; MURAMATSU S
ULSI Device Development Laboratories, Japan
Journal: NEC research & development, 1997, 38 (4) 412-418
Language: English
The influence of phosphorus at the Floating Gate (FG)/tunnel oxide interface on the **FLASH memory** data retention characteristics is investigated. By measuring the electrical characteristics of memory cells and MOS capacitors, a close relationship was found between the memory cell data retention and Stress Induced Leakage Current (SILC). Lowering the phosphorus density in the FG suppresses SILC and prolongs the data retention. Applying amorphous Si (a-Si) to the FG, in addition, is also found to improve SILC. Thus, the memory cell data retention characteristics is expected to be improved when a-Si is applied to the FG. This a-Si FG advantage is investigated by C-V characteristics, SIMS (Secondary Ion Mass Spectroscopy) and EDX (Energy Dispersive X-Ray Spectroscopy) analysis. In spite of the high impurity activation ratio, the phosphorus concentration at the FG/tunnel oxide interface was confirmed to be lower for the a-Si FG than for the poly-Si FG. Applying a-Si therefore, is confirmed to have the same effect as lowering the phosphorus concentration in the FG but preventing the gate depletion effect. This attractive phenomenon for a-Si may be resulting from the lower phosphorus diffusion along the grain boundary. a-Si therefore will be considered as the promising material for high reliability **FLASH memories**.

24/3,AB/48 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

13195511 PASCAL No.: 97-0459787
FLASH memory data retention reliability and the floating gate/tunnel SiO SUB 2 interface characteristics
KUBOTA T; ANDO K; MURAMATSU S
HATTORI Takeo, ed; WADA Kazuhiko, ed; HIRAKI Akio, ed
ULSI Device Development Laboratories, NEC Corporation, 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan
Musashi Institute of Technology, Setagaya-ku, Tokyo 158, Japan; NTT LSI Laboratories, Atsugi, Kanagawa 243-01, Japan; Department of Electrical Engineering, Osaka University, Suita 565, Japan
ISCSI-2: International Symposium on the Control of Semiconductor Interfaces, 2 (Karuizawa JPN) 1996-10-28
Journal: Applied surface science, 1997, 117-18 253-258

Language: English

The influence of phosphorus at the floating gate (FG)/tunnel oxide interface on the **FLASH memory** data retention characteristics is investigated. By measuring the electrical characteristics of memory cells and MOS capacitors, a close relationship was found between the memory cell data retention and stress induced leakage current (SILC). Lowering the phosphorus density in the FG suppresses SILC and prolong the data retention. Applying amorphous Si (a-Si) to the FG, in addition is also found to improve SILC. Thus the memory cell data retention characteristics are expected to be improved when a-Si is applied to the FG. This a-Si FG advantage is investigated by C-V characteristics, SIMS and EDX analysis. In spite of the high impurity activation ratio, the phosphorous concentration at the FG/tunnel oxide interface was confirmed to be lower for the a-Si FG than for the poly-Si FG. Applying a-Si therefore, is confirmed to have the same effect as lowering the phosphorus concentration in the FG but preventing the gate depletion effect. This attractive phenomenon for a-Si may result from the lower phosphorus diffusion along the grain boundary, a-Si therefore is the most promising material for high reliability **FLASH memories**.

24/3,AB/49 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

04093679 GRA-96-21401; EDB-97-002383
Title: Sharp Technical Journal, Volume·61, April 1995
Corporate Source: Sharp Corp., Nara (Japan)
Publication Date: Apr 1995
(83 p)
Report Number(s): PB-96-212659/XAB
Language: English

Abstract: Contents: Present Situation and Trend of Electronic Packaging Technology; Thermal Stabilization Technique of Power HBTs; A Low Noise Fan Operating in Inlet Distortions; Development of 2.4 GHz Low Power Data Communication System; An Automatic Protocol Recognition Scheme of Infrared Communication Protocols; Development of a Three Dimensional Illuminance Analysis System Using Ray Tracing Method; Reliable Red-Emitting Laser Diodes Grown by Solid-Source Molecular Beam Epitaxy; Low Temperature Deposition of High Quality **Silicon Dioxide** Films; Switching Power Supply Simulation by PSpice; Development of MD-DATA Drive Unit; Development of Rehabilitation Software for Cognitive Function Retarded Patients; 'Azayaka Shoin' Japanese Color Word Processor WD-C700; Automatic Washing Machine with Economized Water Mechanism ES-S65; Vacuum Cleaner with Edge Clean Function; 5V Only 16M/8M **Flash Memory**; Primary Regulator for Power Supply.